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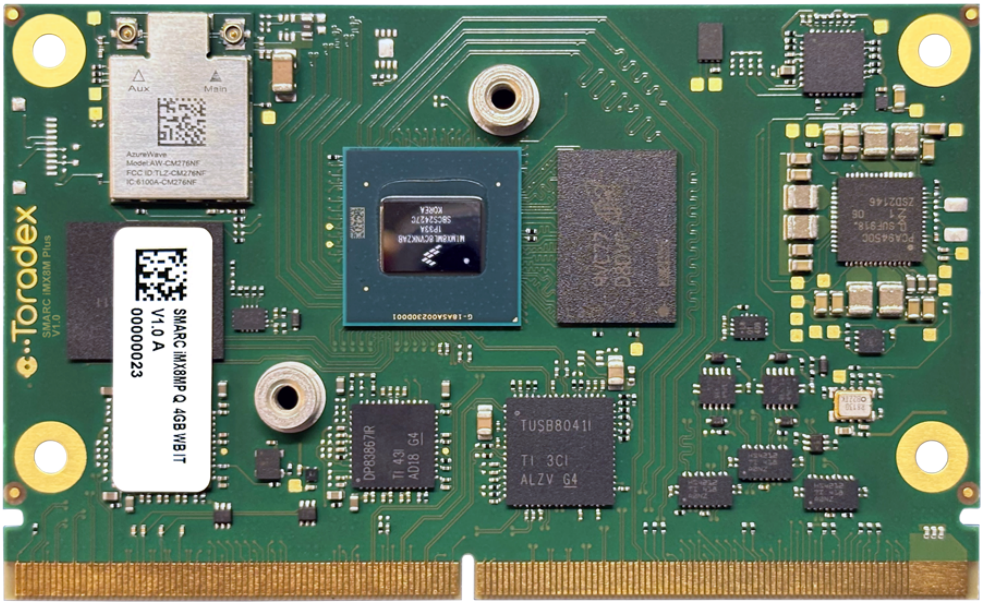
# SMARC i.MX8M Plus

## HW Datasheet

Preliminary – Subject to Change



# Revision History

Document Revisions

| Date | Doc. Revision | Product Version | Changes |
|---|---|---|---|
| 10-Mar-2025 | Rev. 0.1 | V1.0 | Initial documentation |

# Contents

# 1 Introduction

## 1.1 Purpose of the Datasheet

The datasheet represents the hardware capabilities of the SMARC iMX8M Plus. For information on the actual features supported by software, please refer to the relevant SoM product page on the Toradex Developer website: https://developer.toradex.com/hardware/smarc-som-family/modules/smarc-imx8m-plus.

## 1.2 SMARC SoM Family

The Toradex SMARC Family brings the trusted well-known Toradex quality, reliability, and ease-of-use to the SMARC (Smart Mobility Architecture) standard. The Toradex SMARC Module is built according to the latest SMARC 2.2 and is compatible with most SMARC 2.1/2.0 carrier boards.

As a standard designed to accommodate a wide range of ARM and x86 Systems-on-Chip, SMARC made trade-offs to prioritize broad compatibility over cost, size, and performance.

## 1.3 NXP i.MX 8M Plus SoC

The SMARC iMX8M Plus SoM is based on the NXP i.MX 8M Plus family of embedded System on Chips (SoCs). The i.MX 8M Plus family consists of the i.MX 8M Plus Quad, i.MX 8M Plus QuadLite, and i.MX 8M Plus Dual. Section 5 on page 15 gives a detailed information about each of those chips.

The top-tier i.MX 8M Plus Quad features four Arm®Cortex®-A53 cores as the main processor cluster. The cores provide complete 64-bit Arm®v8-A support while maintaining seamless backward compatibility with 32-bit Arm®v7-A software. The main cores run at up to 1.8 GHz for commercial graded products and 1.6 GHz for industrial temperature range products.

In addition to the main CPU complex, the i.MX 8M Plus features a Arm®Cortex®-M7 processor, which peaks up to 800 MHz. This processor is independent of the main complex. However, it has shared access to the peripheral interface. This heterogeneous multicore system allows for running additional real-time operating systems on the M7 cores for time- and security-critical tasks.

Depending on the version, the SoC features a Neural Processing Unit (NPU) with up to 2.3 TOPS that can significantly accelerate machine learning tasks. Some SoC versions also feature a Video Processing Unit (VPU) for accelerating video decoding and encoding. The optional Image Signal Processing (ISP) core accelerates the camera interface by providing a complete video and still picture input block. It features image processing and color space conversion.

The i.MX 8M Plus SoC features inline ECC (error-correcting code) for the LPDDR4 DRAM for high system reliability and safety.

The i.MX 8M Plus Quad features the GC7000 UltraLite 3D Graphics Processing Unit (GPU) from Vivante®. The GPU provides eight Vega shader core which peaks up to 16 GFLOPS and supports OpenGL® ES 3.0, OpenCL™ 1.2, and Vulkan®. In addition to the GPU, the SoC features the GC520L Composition Processing Core (CPC).

The i.MX 8M Plus SoC incorporates DVFS (Dynamic Voltage and Frequency Switching) and thermal throttling, enabling the system to continuously adjust both the operating frequency and the voltage in response to changes in workload and temperature, thus achieving the best performance with the lowest power consumption.

## 1.4 SMARC i.MX 8M Plus SoM

Introducing Toradex SMARC i.MX8M Plus **(compatible with SMARC 2.2)**, a compact, yet powerful, SoM designed to bring exceptional performance, flexibility, and scalability to a variety of embedded applica-

tions.

With SMARC's standard form factor and the NXP i.MX8M Plus's advanced processing, multimedia, and connectivity capabilities, this SoM is ideal for industrial automation, edge computing, IoT devices, and smart applications. The i.MX8M Plus integrates a quad-core Arm Cortex-A53 CPU, a dedicated NPU (in the 4GB model), and multimedia features like hardware-accelerated video decoding and encoding, ensuring robust and efficient operation for a wide range of use cases.

# 2 Main Features

## 2.1 CPU

Table 1: CPU features

| Parameter | SMARC i.MX8M Plus Quad 4GB WB IT |
|---|---|
| SoC | MIMX8ML8CVNKZAB |
| A53 Cores | 4 |
| M7 Cores | 1 |
| CPU Clock | A53: 1600MHz<br>M7: 800MHz |
| L1 Instruction Cache<br>*per core* | A53: 32 kB<br>M7: 32 kB |
| L1 Data Cache<br>*each core* | A53: 32 kB<br>M7: 32 kB |
| L2 Cache<br>*shared* | A53: 512 kB |
| Tightly Coupled Memory | M7: 256 kB |
| Maximum CPU frequency | A53: 1.6 GHz<br>M7: 800 MHz |
| Arm® Neon™ MPE | Yes |
| NPU | Yes |
| NPU Performance | 2.3 TOP/s |
| ISP | Yes |
| ISP Performance | 375 Mpixel/s HDR |
| VPU | Yes |
| Resource Domain Controller | Yes |
| Arm® TrustZone® | Yes |
| High Assurance Boot | Yes |
| Cryptographic Acceleration and Assurance Module | Yes |
| Secure Real-Time Clock | Yes |
| Secure JTAG Controller | Yes |
| Secure Non-Volatile Storage† | Yes |

† Secure Non-Volatile Storage (SNVS) runs from the main VCC, not the VCC_BACKUP. Therefore, it can only be used if VCC is permanently applied to the module.

## 2.2 GPU

Table 2: GPU Features

| Parameter | Verdin iMX8M Plus Quad 4GB WB IT |
|---|---|
| Vivante GC7000UL GPU Units | 1 |
| Vega Shader cores | 8 |

*Continued on next page*

Table 2: GPU Features (Continued)

| Parameter | Verdin iMX8M Plus Quad 4GB WB IT |
|---|---|
| OpenGL® ES 3.0, 2.0, 1.1 | Yes |
| OpenGL® 3.0, 2.1 | Yes |
| OpenVG™ 1.1 | Yes |
| OpenCL™ 1.2 | Yes |
| Vulkan | Yes |
| GC520L CPC Units | 1 |

## 2.3 Interfaces

Table 3: Interfaces Features

| Parameter | Verdin iMX8M Plus Quad 4GB WB IT |
|---|---|
| **Audio** | |
| Digital Audio | 2x I²S |
| **Camera** | |
| MIPI® CSI-2 | 1x Quad Lane + 1x Dual Lane |
| **Display** | |
| Display Controllers | Triple |
| HDMI<br>*2.0a* | 1x (up to 4K) |
| LVDS<br>*1x dual-channel* | 1x (up to 1920x1080) |
| MIPI® DSI | 1x Quad Lane |
| **Low Speed** | |
| CAN-FD | 2 |
| GPIO | 14 |
| I²C | 4 |
| PWM | 1 |
| SPI | 2 |
| UART | 4 |
| **Network** | |
| Bluetooth | Classic / LE 5.3 |
| Ethernet | 2x Gigabit |
| Wi-Fi | 2.4/5 GHz Dual Band 2x2<br>Wi-Fi 5 (802.11ac) |
| **Other** | |
| PCIe<br>*Gen 3* | 1 |
| **Storage** | |

*Continued on next page*

Table 3: Interfaces Features (Continued)

| Parameter | Verdin iMX8M Plus Quad 4GB WB IT |
|---|---|
| SD/SDIO/MMC | 1 |
| **USB** | |
| USB 2.0 (Host) | 5 |
| USB 3.1 (Gen 1 OTG) | 2 |

## 2.4 Memory

Table 4: Memory Features

| Parameter | Verdin iMX8M Plus Quad 4GB WB IT |
|---|---|
| **eMMC** | |
| eMMC Configuration | 3D TLC |
| eMMC Capacity | 32 GB |
| **I²C EEPROM** | |
| I²C EEPROM Capacity | 2 kbit<br>256 × 8bit |
| I²C EEPROM Bus Speed | **Fast:** 400kHz<br>**Std.:** 100 kHz |
| **RAM** | |
| RAM Capacity | 4 GB<br>*Dual-rank* |
| RAM Configuration<br>*Ctrl. × Ch. × bpc*[1] | 32 bits<br>*1 × 2 × 16* |
| RAM Type | LPDDR4 |
| RAM Speed | 4000 MT/s<br>*2 GHz* |
| Inline ECC | Yes |

[1] Controllers × Channels per controller × bits per channel.
[2] eMMC is based on MLC or TLC NAND flash memory. As with all flash memories, the write endurance is limited. Extensive writing to the memory can wear out the memory cell. The wear leveling in the eMMC controller helps to ensure that cells are getting worn out evenly. More information can be found here https://developer.toradex.com/hardware/hardware-resources/flash-memory-overview-on-toradex-products.

## 2.5 Physical

Table 5: Physical Features

| Parameter | Verdin iMX8M Plus Quad 4GB WB IT |
|---|---|
| Module dimensions | 82.0 × 50.0 mm |
| Temperature range | -40 °C to +85 °C[†] |

*Continued on next page*

Table 5: Physical Features (Continued)

| Parameter | Verdin iMX8M Plus Quad 4GB WB IT |
|---|---|
| Shock / Vibration | EN 60068-2-6/50g 20 ms |
| Power dissipation | TBD |

† The Wi-Fi/Bluetooth module featured on the SoM has been validated for an operating temperature range of -30 °C to 85 °C. The rest of the components are rated and have been validated for the complete -40 °C to 85 °C temperature range.

# 3 Interface Overview

Table 6: Interfaces Overview

| Feature | Sub Feature | SMARC Spec | Toradex SMARC i.MX8M Plus | Comments |
|---|---|---|---|---|
| Wireless Module | It is optional, shows if option is available | May | Yes | Build-to-Order (BTO) options without Wi-fi |
| Size | 82 x 50 mm | Shall | Yes | |
| | 82 x 80 mm | May | Not Available | Unavailable |
| LVDS LCD | LVDS0 18/24 bit single channel | Should | Yes | Muxed with DSI0 (4 lanes) |
| | LVDS1 24 bit single channel | May | Yes | |
| eDP on LVDS Pins | eDP0 on LVDS0 - 4 diff pairs | May | Not Available | |
| | eDP1 on LVDS1 - 4 diff pairs | May | Not Available | |
| DSI on LVDS Pins | DSI0-2 lane implementation | May | Not Available | |
| | DSI0-4 lane implementation | May | Yes | Assembly option. Muxed with LVDS |
| | DSI1-2 lane implementation | May | Not Available | |
| | DSI1-4 lane implementation | May | Not Available | |
| HDMI | HDMI Display interface | Should | Yes | HDMI 2.0a up to 4K30 (3840x2160@30Hz) |
| DP on HDMI Pins | | May | Not Available | |
| DP++ | DisplayPort++ | May | Not Available | |
| CSI | CSI0 - 2 lane | May | Yes | |
| | CSI1 - 2 lane implementation | Should | Yes | |
| | CSI1 - 4 lane implementation | Should | Yes | |
| | CSI2 - 2 lane implementation | May | Not Available | |
| | CSI2 - 4 lane implementation | May | Not Available | |
| | CSI3 - 2 lane implementation | May | Not Available | |
| | CSI3 - 4 lane implementation | May | Not Available | |
| SDIO | SDIO (4 bit, for SD cards) | Should | Yes | |
| SPI | SPI0 | Should | Yes | ECSPI1 |
| | SPI1 | Should | Yes | ECSPI2 |
| | QuadSPI | Should | Not Available | |
| | eSPI | Should | Not Available | |
| Audio | I2S0 | Should | Yes | |
| | HDA or I2S2 | Should | Yes(I2S2) | |
| I2C | Power Management | Shall | Yes | PMIC_I2C |
| | General Purpose | Shall | Yes | I2C_1 |
| | Camera 0/1/2/3 | Should | Yes | I2C_4_CSI |
| | LCD Display I/D | Should | Yes | I2C_2_DSI |
| | HDMI | Should | Yes | I2C_3_HDMI |
| Serial Ports | SER0 (4 wire) | Shall | Yes | Console output is acceptable on SER1 and SER3. |
| | SER1 (2 wire) | Shall | Yes | |
| | SER2 (4 wire) | Should | Yes | |

*Continued on next page*

Table 6: Interfaces Overview (Continued)

| Feature | Sub Feature | SMARC Spec | Toradex SMARC i.MX8M Plus | Comments |
|---|---|---|---|---|
| | SER3 (2 wire) | Should | Yes | |
| CAN | CAN0 | May | Yes | |
| | CAN1 | May | Yes | |
| USB | USB0 (2.0) OTG | Shall | Yes | |
| | USB1 (2.0) | Should | Yes | Assembly option: USB Hub |
| | USB2 (2.0) | May | Yes | |
| | USB2 (3.2) - Additional SS signals | Should | Yes | |
| | USB3 (2.0) | May | Yes | Assembly option: USB Hub |
| | USB3 (3.2) - Additional SS signals | May | Yes | Assembly option: USB Hub |
| | USB4 (2.0) | May | Yes | Assembly option: USB Hub |
| | USB5 (2.0) | May | Not Available | |
| PCIe | PCIE_A (x1 Gen 1 Root) | Should | Yes | PCIe x1 Gen 3 |
| | PCIE_B (x1 Gen 1 Root) | May | Not Available | |
| | PCIE_C (x1 Gen 1 Root) | May | Not Available | |
| | PCIE_D (x1 Gen 1 Root) | May | Not Available | |
| SERDES | Alternative use of PCIE_C and/or PCIE_D | May | Not Available | |
| SATA | SATA Gen 1 | Should | Not Available | |
| | SATA Gen 2 operation | May | Not Available | |
| | SATA Gen 3 operation | May | Not Available | |
| GbE | GBE0 | Should | Yes | Ethernet PHYs on SoM |
| | GBE1 | May | Yes | Ethernet PHYs on SoM |
| | IEEE1588 Triggers(GBE[0:1]_SDP) | May | Yes | |
| Watchdog | WDT Out | Should | Yes | |
| GPIO | GPIO[0:11] | Shall | Yes | GPIO expander |
| | GPIO[12:13] | Should | Yes | |
| | GPIO[0:11] interrupt capability | Shall | Yes | |
| | GPIO[12:13] interrupt capability | Should | Yes | |
| | GPIO Camera Support | Shall | Yes | |
| | GPIO5 PWM capability | Should | Yes | |
| | GPIO6 Tachin capability | Should | Yes | |
| Management | System and power management features | Shall | Yes | Implemented according to SMARC V2.2 Specifications |
| | BATLOW# | Shall | Yes | |
| | CARRIER_PWR_ON | Shall | Yes | |
| | CARRIER_STBY# | Should | Yes | |
| | CHARGER_PRSNT# | Should | Yes | |
| | CHARGING# | Should | Yes | |
| | VIN_PWR_BAD# | Should | Yes | |

*Continued on next page*

Table 6: Interfaces Overview (Continued)

| Feature | Sub Feature | SMARC Spec | Toradex SMARC i.MX8M Plus | Comments |
|---|---|---|---|---|
| Management | SLEEP# | Should | Yes | |
| | LID# | Should | Yes | |
| | POWER_BTN# | Should | Yes | |
| | RESET_OUT# | Should | Yes | |
| | RESET_IN# | Should | Yes | |
| | SMB_ALERT# | Should | Yes | |
| | TEST# | Should | Yes | |
| Boot Select | BOOT_SEL0#<br>nBOOT_SEL1#<br>nBOOT_SEL2# | Shall | Yes | Implemented according to SMARC V2.2 Specifications. Boot sources supported: Carrier SD Card (SDIO interface), Module eMMC Flash, Remote boot (GBE, serial) |
| Force Recovery | FORCE_RECOV | Shall | Yes | Implemented according to SMARC V2.2 Specifications |
| JTAG | JTAG Connector on Module | May | Yes | Assembly option - assembled on samples |
| RTC | | Should | Yes | VDD_RTC |

*Note*: Data provided is based on the latest available specifications.

# 4 Reference Documents

## 4.1 EEPROM

The SMARC iMX8M Plus has an on-module $I^2C$ EEPROM, the M24C02 from STMicroelectronics.
https://www.st.com/en/memories/m24c02-r.html

## 4.2 PCB Temperature Sensor

The SMARC iMX8M Plus can be assembled with a PCB temperature sensor, the TMP1075DSGR from TI.
https://www.ti.com/lit/gpn/tmp1075

## 4.3 Ethernet Transceiver

SMARC iMX8M Plus utilizes a Texas Instruments DP83867IRRGZR Gigabit Ethernet Transceiver (PHY) with RGMII.
https://www.ti.com/product/DP83867IR/part-details/DP83867IRRGZR

## 4.4 NXP i.MX 8M Plus

You will find additional details about the i.MX 8M Plus SoC in the Datasheet and Reference Manual provided by NXP.
https://www.nxp.com/products/processors-and-microcontrollers/arm-processors/i-mx-applications-processors/i-mx-8-processors/i-mx-8m-plus-arm-cortex-a53-machine-learning-vision-multimedia-and-industrial-iot:IMX8MPLUS

## 4.5 Layout Design Guide

This document contains information about high-speed layout design and additional factors that help get the carrier board layout right the first time.
https://docs.toradex.com/102492-layout-design-guide.pdf

## 4.6 RTC

The SMARC iMX8M Plus has a low-power RX8130CE real-time clock from Epson.
https://www5.epsondevice.com/en/products/rtc/rx8130ce.html

## 4.7 SMARC Specification

The SMARC iMX8M Plus follows the SMARC 2.2 spefication.

- SMARC Hardware Specification 2.2
- SMARC Design Guide 2.1.1

## 4.8 SMARC Carrier Board Schematics

We provide complete schematics plus an Altium project file that includes library symbols and IPC-7351 compliant footprints for the SMARC Development Board and other carrier boards, free of charge. This resource is of great help when designing your own carrier board.
https://developer.toradex.com/carrier-board-design/reference-designs

## 4.9 Toradex Developer Center

The Toradex Developer Center is updated with the latest product support information regularly. You can find an abundance of additional information there.

Please note that the Developer Center is shared across all Toradex products. You should always check to ensure that the information provided is valid and relevant for the SMARC iMX8M Plus.
https://developer.toradex.com/

## 4.10 Wi-Fi and Bluetooth Module

Some SMARC iMX8M Plus models utilize an AzureWave AW-CM276NF wireless module. The AW-CM276NF datasheet is available from AzureWave.
https://www.azurewave.com/wireless-modules-nxp.html

Information on pre-certified antennas and cables can be found here:
https://developer.toradex.com/knowledge-base/wi-fi-accessories-recommended-for-toradex-products

Certification documents are available on the Toradex website:
https://developer.toradex.com/knowledge-base/certification-documents-for-azurewave-aw-cm276nf-wi-fi-bluetooth-module

# 5 Naming Conventions

The naming of i.MX 8M Plus based products can be confusing. In this document, a consistent naming convention is used. It is essential to notice the punctuation and spaces in the names. Do not confuse:

- The i.MX 8M Plus, the i.MX 8 or the i.MX 8M. These are three different SoC families with different features.
- The **SMARC** i.MX 8M Plus or the **SMARC** i.MX 8M Plus. These are three different SoM families with different features.

## 5.1 Naming of NXP System on Chip

Table 7: Naming of NXP System on Chip

| NXP System on Chip | Description |
|---|---|
| i.MX 8 Series | A series of different SoC families which consist of the i.MX 8, i.MX8M, i.MX 8M Plus, i.MX 8M Mini, i.MX 8M Nano, as well as the i.MX 8X families. This document only contains information on the SMARC module, which uses an i.MX 8M Plus family SoC. For information on other i.MX 8 Series based modules, please visit the Toradex website. |
| i.MX 8M Plus | The NXP i.MX 8M Plus SoC family, which consists of the i.MX 8M Plus Quad, i.MX 8M Plus Quad Lite, and i.MX 8M Plus Dual. Whenever this document uses the term i.MX 8M Plus, all versions of the i.MX 8M Plus SoC family are meant. |
| i.MX 8MP | Short name for the i.MX 8M Plus SoC family. |
| i.MX 8M Plus Quad | The top-tier SoC of the i.MX 8M Plus family. It features a quad-core Cortex-A53 main CPU with VPU, ISP, and an optional NPU. |
| i.MX 8MPQ | Short name for the i.MX 8M Plus Quad. |
| i.MX 8M Plus Quad Lite | Quad-Core SoC of the i.MX 8M Plus family, which does not include the VPU, NPU, and ISP. |
| i.MX 8MPQL | Short name for the i.MX 8M Plus Quad Lite. |
| i.MX 8M Plus Dual | Dual Core Cortex-A53 version of the i.MX 8M Plus family. It contains VPU, NPU, and ISP. |
| i.MX 8MPD | Short name for the i.MX 8M Plus Dual. |

## 5.2 Naming of Toradex Modules

Table 8: Naming of Toradex Modules

| Toradex Module | Description |
|---|---|
| SMARC iMX8M Plus | SMARC module based on the i.MX 8M Plus family SoC. Whenever this document uses the term SMARC iMX8M Plus, all versions of the SMARC iMX8MP are meant. |
| SMARC iMX8MP | Short name for the SMARC iMX8M Plus. Whenever this document uses the term SMARC iMX8MP, all versions of the SMARC iMX8M Plus are meant. |
| SMARC iMX8M Plus Quad 4GB WB IT | SMARC module based on the i.MX 8M Plus Quad processor with 4GB memory, Wi-Fi and Bluetooth function, and Industrial Temperature (IT) range. |
| SMARC iMX8MP Q 4GB WB IT | Short name for the SMARC iMX8M Plus Quad 4GB WB IT. |
| Verdin iMX8M Plus | Verdin module based on the i.MX 8M Plus family SoC. This document only contains information on the SMARC module. For information on other i.MX 8 Series based modules, please visit the Toradex website. |

# 6 Build-To-Order Options

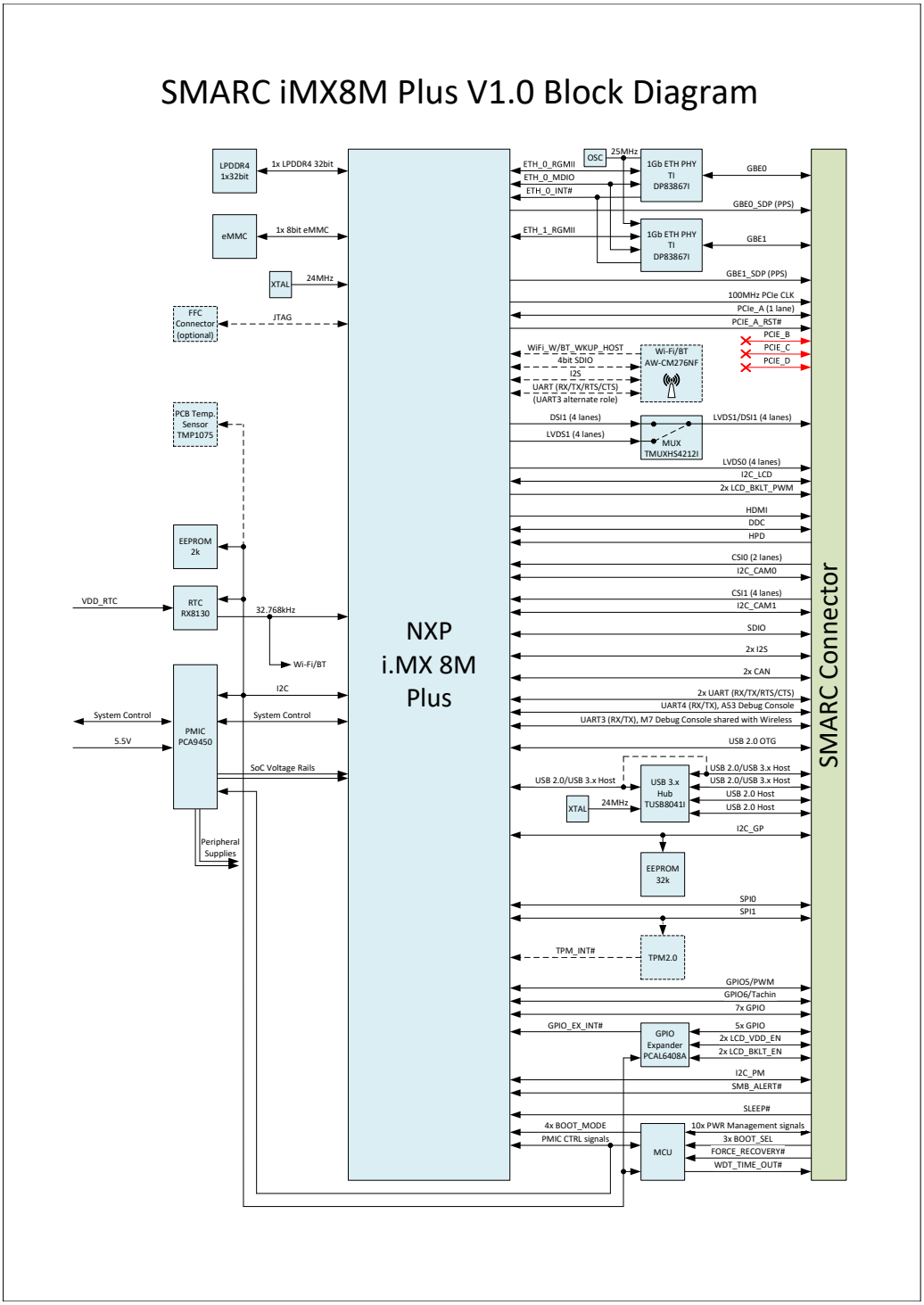
It is possible to order customized versions of this module. These versions are Build-To-Order (BTO). The following customization options are available for Toradex SMARC i.MX8M Plus:

- Connectivity
  - Options without WiFi/BT module
  - Options without Ethernet PHY(s)
- Memory
  - RAM Density (1-8GB)
  - eMMC Capacity (8-128GB)
  - EEPROM Capacity
- Temperature Range
  - Commercial : 0°C - 70°C
  - Wide Temp : -25°C - 85°C
  - Industrial : -40°C - 85°C
- TPM 2.0 (on SPI or I2C interface)

# 7 Architecture Overview

## 7.1 Block Diagram

Figure 1: Block Diagram



# 8 SMARC i.MX 8M Plus Connector

## 8.1 Pin Numbering

The SMARC module follows the same pin numbering scheme defined by the SMARC standard (Section 4.7). Pins on the top side (primary) of the module are numbered from P1 to P156, while the pins on the bottom side (secondary) are numbered from S1 to S158. The key pins are not numbered.

## 8.2 Pin Assignment

Table 9: X1 pin assignment – top side – Primary pins Secondary pins – Alternate functions

| MXM3 Pins | Signal Group | SMARC Signal | Soc Signal | Soc Ball Name | Power Group | Note |
|---|---|---|---|---|---|---|
| P1 | CTRL | SMB_ALERT# | NAND_READY_B | T28 | NVCC_NAND | |
| P2 | CTRL | GND | _GND | | | |
| P3 | CSI | CSI1_CK+ | MIPI_CSI1_CLK_P | D22 | VDD_MIPI_0P8 | |
| P4 | CSI | CSI1_CK- | MIPI_CSI1_CLK_N | E22 | VDD_MIPI_0P8 | |
| P5 | Ethernet | GBE1_SDP | SAI1_RXC | AH8 | NVCC_SAI1_SAI5 | Level Shifted - Output - CMOS - IC |
| P6 | Ethernet | GBE0_SDP | GPIO1_IO09 | B8 | NVCC_GPIO1 | Level Shifted - Output - CMOS - IC |
| P7 | CSI | CSI1_RX0+ | MIPI_CSI1_D0_P | D18 | VDD_MIPI_0P8 | |
| P8 | CSI | CSI1_RX0- | MIPI_CSI1_D0_N | E18 | VDD_MIPI_0P8 | |
| P9 | CSI | GND | _GND | | | |
| P10 | CSI | CSI1_RX1+ | MIPI_CSI1_D1_P | D20 | VDD_MIPI_0P8 | |
| P11 | CSI | CSI1_RX1- | MIPI_CSI1_D1_N | E20 | VDD_MIPI_0P8 | |
| P12 | CSI | GND | _GND | | | |
| P13 | CSI | CSI1_RX2+ | MIPI_CSI1_D2_P | D24 | VDD_MIPI_0P8 | |
| P14 | CSI | CSI1_RX2- | MIPI_CSI1_D2_N | E24 | VDD_MIPI_0P8 | |
| P15 | CSI | GND | _GND | | | |
| P16 | CSI | CSI1_RX3+ | MIPI_CSI1_D3_P | D26 | VDD_MIPI_0P8 | |
| P17 | CSI | CSI1_RX3- | MIPI_CSI1_D3_N | E26 | VDD_MIPI_0P8 | |
| P18 | CSI | GND | _GND | | | |
| P19 | Ethernet | GBE0_MDI3- | ETH_0 PHY | | | |
| P20 | Ethernet | GBE0_MDI3+ | ETH_0 PHY | | | |
| P21 | Ethernet | GBE0_LINK_MID# | ETH_0 PHY | | | Level Shifted - MOSFET - Output - OD |
| P22 | Ethernet | GBE0_LINK_MAX# | ETH_0 PHY | | | Level Shifted - MOSFET - Output - OD |
| P23 | Ethernet | GBE0_MDI2- | ETH_0 PHY | | | |

*Continued on next page*

Table 9: X1 pin assignment – top side – Primary pins Secondary pins – Alternate functions (Continued)

| MXM3 Pins | Signal Group | SMARC Signal | Soc Signal | Soc Ball Name | Power Group | Note |
|---|---|---|---|---|---|---|
| P24 | Ethernet | GBE0_MDI2+ | ETH_0 PHY | | | |
| P25 | Ethernet | GBE0_LINK_ACT# | ETH_0 PHY | | | Level Shifted - MOSFET - Output - OD |
| P26 | Ethernet | GBE0_MDI1- | ETH_0 PHY | | | |
| P27 | Ethernet | GBE0_MDI1+ | ETH_0 PHY | | | |
| P28 | Ethernet | GBE0_CTREF | | Not Connected | | |
| P29 | Ethernet | GBE0_MDI0- | ETH_0 PHY | | | |
| P30 | Ethernet | GBE0_MDI0+ | ETH_0 PHY | | | |
| P31 | SPI | SPI0_CS1# | SAI3_RXFS | AJ19 | NVCC_SAI2_SAI3_SPDIF | |
| P32 | SPI | GND | _GND | | | |
| P33 | SDIO | SDIO_WP | SD2_WP | AC26 | NVCC_SD2 | |
| P34 | SDIO | SDIO_CMD | SD2_CMD | AB28 | NVCC_SD2 | |
| P35 | SDIO | SDIO_CD# | SD2_CD_B | AD29 | NVCC_SD2 | |
| P36 | SDIO | SDIO_CK | SD2_CLK | AB29 | NVCC_SD2 | |
| P37 | SDIO | SDIO_PWR_EN | SD2_RESET_B | AD28 | NVCC_SD2 | Level Shifted - Output - CMOS - IC |
| P38 | SDIO | GND | _GND | | | |
| P39 | SDIO | SDIO_D0 | SD2_DATA0 | AC28 | NVCC_SD2 | |
| P40 | SDIO | SDIO_D1 | SD2_DATA1 | AC29 | NVCC_SD2 | |
| P41 | SDIO | SDIO_D2 | SD2_DATA2 | AA26 | NVCC_SD2 | |
| P42 | SDIO | SDIO_D3 | SD2_DATA3 | AA25 | NVCC_SD2 | |
| P43 | SPI | SPI0_CS0# | ECSPI1_SS0 | AE20 | NVCC_ECSPI_HDMI | |
| P44 | SPI | SPI0_CK | ECSPI1_SCLK | AF20 | NVCC_ECSPI_HDMI | |
| P45 | SPI | SPI0_DIN | ECSPI1_MISO | AD20 | NVCC_ECSPI_HDMI | |
| P46 | SPI | SPI0_DO | ECSPI1_MOSI | AC20 | NVCC_ECSPI_HDMI | |

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Table 9: X1 pin assignment – top side – Primary pins Secondary pins – Alternate functions (Continued)

| MXM3 Pins | Signal Group | SMARC Signal | Soc Signal | Soc Ball Name | Power Group | Note |
|---|---|---|---|---|---|---|
| P47 | SPI | GND | _GND | | | |
| P48 | SATA | SATA_TX+ | | Not Connected | | |
| P49 | SATA | SATA_TX- | | Not Connected | | |
| P50 | SATA | GND | _GND | | | |
| P51 | SATA | SATA_RX+ | | Not Connected | | |
| P52 | SATA | SATA_RX- | | Not Connected | | |
| P53 | SATA | GND | _GND | | | |
| P54 | QSPI | ESPI_CS0# / SPI1_CS0# / QSPI_CS0# | ECSPI2_SS0 | AJ22 | NVCC_ECSPI_HDMI | |
| P55 | QSPI | ESPI_CS1# / SPI1_CS1# / QSPI_CS1# | SAI1_RXD1 | AF10 | NVCC_SAI1_SAI5 | |
| P56 | QSPI | ESPI_CK / SPI1_CK / QSPI_CK | ECSPI2_SCLK | AH21 | NVCC_ECSPI_HDMI | |
| P57 | QSPI | ESPI_IO_1 / SPI1_DIN / QSPI_IO_1 | ECSPI2_MISO | AH20 | NVCC_ECSPI_HDMI | |
| P58 | QSPI | ESPI_IO_0 / SPI1_DO / QSPI_IO_0 | ECSPI2_MOSI | AJ21 | NVCC_ECSPI_HDMI | |
| P59 | QSPI | GND | _GND | | | |
| P60 | USB | USB0+ | USB1_D_P | D10 | VDD_USB_3P3 | |
| P61 | USB | USB0- | USB1_D_N | E10 | VDD_USB_3P3 | |
| P62 | USB | USB0_EN_OC# | GPIO1_IO12 | A5 | NVCC_GPIO1 | Level Shifted - MOSFET - Output - OD |
| P63 | USB | USB0_VBUS_DET | USB1_VBUS | A11 | VDD_USB_3P3 | 5V Capable |
| P64 | USB | USB0_OTG_ID | SAI3_MCLK | AJ20 | NVCC_SAI2_SAI3_SPDIF | |
| P65 | USB | USB1+ | USB_Hub | | | |
| P66 | USB | USB1- | USB_Hub | | | |
| P67 | USB | USB1_EN_OC# | USB_Hub | | | Level Shifted - MOSFET - Output - OD |
| P68 | USB | GND | _GND | | | |
| P69 | USB | USB2+ | USB_Hub | | | |

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Table 9: X1 pin assignment – top side – Primary pins Secondary pins – Alternate functions (Continued)

| MXM3 Pins | Signal Group | SMARC Signal | Soc Signal | Soc Ball Name | Power Group | Note |
|---|---|---|---|---|---|---|
| P70 | USB | USB2- | USB_Hub | | | |
| P71 | USB | USB2_EN_OC# | USB_Hub | | | Level Shifted - MOSFET - Output - OD |
| P72 | USB | RSVD | | Not Connected | | |
| P73 | USB | RSVD | | Not Connected | | |
| P74 | USB | USB3_EN_OC# | USB_Hub | | | Level Shifted - MOSFET - Output - OD |
| key | | | | | | |
| key | | | | | | |
| key | | | | | | |
| key | | | | | | |
| P75 | PCIe | PCIE_A_RST# | SAI1_TXD7 | AJ13 | NVCC_SAI1_SAI5 | Level Shifted - MOSFET - Output - OD |
| P76 | PCIe | USB4_EN_OC# | USB_Hub | | | Level Shifted - MOSFET - Output - OD |
| P77 | PCIe | PCIE_B_CKREQ# | | Not Connected | | |
| P78 | PCIe | PCIE_A_CKREQ# | | Not Connected | | |
| P79 | PCIe | GND | _GND | | | |
| P80 | PCIe | PCIE_C_REFCK+ | | Not Connected | | |
| P81 | PCIe | PCIE_C_REFCK- | | Not Connected | | |
| P82 | PCIe | GND | _GND | | | |
| P83 | PCIe | PCIE_A_REFCK+ | PCIE_REF_PAD_CLK_P | D16 | PCIE_VDDH_CMN | |
| P84 | PCIe | PCIE_A_REFCK- | PCIE_REF_PAD_CLK_N | E16 | PCIE_VDDH_CMN | |
| P85 | PCIe | GND | _GND | | | |
| P86 | PCIe | PCIE_A_RX+ | PCIE_RXN_P | A14 | PCIE_VDDH_CH0 | |
| P87 | PCIe | PCIE_A_RX- | PCIE_RXN_N | B14 | PCIE_VDDH_CH0 | |
| P88 | PCIe | GND | _GND | | | |

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Table 9: X1 pin assignment – top side – Primary pins Secondary pins – Alternate functions (Continued)

| MXM3 Pins | Signal Group | SMARC Signal | Soc Signal | Soc Ball Name | Power Group | Note |
|---|---|---|---|---|---|---|
| P89 | PCIe | PCIE_A_TX+ | PCIE_TXN_P | A15 | PCIE_VDDH_CH0 | |
| P90 | PCIe | PCIE_A_TX- | PCIE_TXN_N | B15 | PCIE_VDDH_CH0 | |
| P91 | HDMI/DP | GND | _GND | | | |
| P92 | HDMI/DP | HDMI_D2+ / DP1_LANE0+ | HDMI_TXD2_P | | | |
| P93 | HDMI/DP | HDMI_D2- / DP1_LANE0- | HDMI_TXD2_N | | | |
| P94 | HDMI/DP | GND | _GND | | | |
| P95 | HDMI/DP | HDMI_D1+ / DP1_LANE1+ | HDMI_TXD1_P | | | |
| P96 | HDMI/DP | HDMI_D1- / DP1_LANE1- | HDMI_TXD1_N | | | |
| P97 | HDMI/DP | GND | _GND | | | |
| P98 | HDMI/DP | HDMI_D0+ / DP1_LANE2+ | HDMI_TXD0_P | | | |
| P99 | HDMI/DP | HDMI_D0- / DP1_LANE2- | HDMI_TXD0_N | | | |
| P100 | HDMI/DP | GND | _GND | | | |
| P101 | HDMI/DP | HDMI_CK+ / DP1_LANE3+ | HDMI_TXC_P | | | |
| P102 | HDMI/DP | HDMI_CK- / DP1_LANE3- | HDMI_TXC_N | | | |
| P103 | HDMI/DP | GND | _GND | | | |
| P104 | HDMI/DP | HDMI_HPD / DP1_HPD | HDMI_HPD | AE22 | NVCC_ECSPI_HDMI | |
| P105 | HDMI/DP | HDMI_CTRL_CK / DP1_AUX+ | HDMI_DDC_SCL | AC22 | NVCC_ECSPI_HDMI | |
| P106 | HDMI/DP | HDMI_CTRL_DAT / DP1_AUX- | HDMI_DDC_SDA | AF22 | NVCC_ECSPI_HDMI | |
| P107 | HDMI/DP | DP1_AUX_SEL | | Not Connected | | |
| P108 | GPIO | GPIO0 / CAM0_PWR# | GPIO_Expander | | | |
| P109 | GPIO | GPIO1 / CAM1_PWR# | GPIO_Expander | | | |
| P110 | GPIO | GPIO2 / CAM0_RST# | GPIO_Expander | | | |
| P111 | GPIO | GPIO3 / CAM1_RST# | GPIO_Expander | | | |

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Table 9: X1 pin assignment – top side – Primary pins Secondary pins – Alternate functions (Continued)

| MXM3 Pins | Signal Group | SMARC Signal | Soc Signal | Soc Ball Name | Power Group | Note |
|---|---|---|---|---|---|---|
| P112 | GPIO | GPIO4 / HDA_RST# | SAI1_TXD6 | AC12 | NVCC_SAI1_SAI5 | |
| P113 | GPIO | GPIO5 / PWM_OUT | GPIO1_IO10 | B7 | NVCC_GPIO1 | |
| P114 | GPIO | GPIO6 / TACHIN | SAI3_RXC | AJ18 | NVCC_SAI2_SAI3_SPDIF | Alternate Function: GPT1_CLK |
| P115 | GPIO | GPIO7 | GPIO1_IO00 | A7 | NVCC_GPIO1 | |
| P116 | GPIO | GPIO8 | GPIO1_IO01 | E8 | NVCC_GPIO1 | |
| P117 | GPIO | GPIO9 | GPIO1_IO05 | B4 | NVCC_GPIO1 | |
| P118 | GPIO | GPIO10 | GPIO1_IO06 | A3 | NVCC_GPIO1 | |
| P119 | GPIO | GPIO11 | GPIO1_IO07 | F6 | NVCC_GPIO1 | |
| P120 | I2C | GND | _GND | | | |
| P121 | I2C | I2C_PM_CK | HDMI_CEC | AD22 | NVCC_ECSPI_HDMI | |
| P122 | I2C | I2C_PM_DAT | SAI5_RXC | AD14 | NVCC_SAI1_SAI5 | |
| P123 | CTRL | BOOT_SEL0# | MCU | | | |
| P124 | CTRL | BOOT_SEL1# | MCU | | | |
| P125 | CTRL | BOOT_SEL2# | MCU | | | |
| P126 | CTRL | RESET_OUT# | MCU | | | |
| P127 | CTRL | RESET_IN# | MCU | | | |
| P128 | CTRL | POWER_BTN# | MCU+SoC | | | |
| P129 | UART | SER0_TX | UART1_TXD | AJ3 | NVCC_I2C_UART | |
| P130 | UART | SER0_RX | UART1_RXD | AD6 | NVCC_I2C_UART | |
| P131 | UART | SER0_RTS# | SAI2_TXFS | AJ17 | NVCC_SAI2_SAI3_SPDIF | |
| P132 | UART | SER0_CTS# | SAI2_RXD0 | AJ14 | NVCC_SAI2_SAI3_SPDIF | |
| P133 | UART | GND | _GND | | | |
| P134 | UART | SER1_TX | UART4_TXD | AH5 | NVCC_I2C_UART | |

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Table 9: X1 pin assignment – top side – Primary pins Secondary pins – Alternate functions (Continued)

| MXM3 Pins | Signal Group | SMARC Signal | Soc Signal | Soc Ball Name | Power Group | Note |
|---|---|---|---|---|---|---|
| P135 | UART | SER1_RX | UART4_RXD | AJ5 | NVCC_I2C_UART | |
| P136 | UART | SER2_TX | UART2_TXD | AH4 | NVCC_I2C_UART | |
| P137 | UART | SER2_RX | UART2_RXD | AF6 | NVCC_I2C_UART | |
| P138 | UART | SER2_RTS# | SD1_DATA5 | AA29 | NVCC_SD1 | |
| P139 | UART | SER2_CTS# | SD1_DATA4 | U26 | NVCC_SD1 | |
| P140 | UART | SER3_TX | UART3_TXD | AJ4 | NVCC_I2C_UART | |
| P141 | UART | SER3_RX | UART3_RXD | AE6 | NVCC_I2C_UART | |
| P142 | UART | GND | _GND | | | |
| P143 | CAN | CAN0_TX | SAI2_TXD0 | AH16 | NVCC_SAI2_SAI3_SPDIF | |
| P144 | CAN | CAN0_RX | SAI2_MCLK | AJ15 | NVCC_SAI2_SAI3_SPDIF | |
| P145 | CAN | CAN1_TX | SAI2_RXC | AJ16 | NVCC_SAI2_SAI3_SPDIF | |
| P146 | CAN | CAN1_RX | SAI2_TXC | AH15 | NVCC_SAI2_SAI3_SPDIF | |
| P147 | PWR | VDD_IN | _VCC | | | |
| P148 | PWR | VDD_IN | _VCC | | | |
| P149 | PWR | VDD_IN | _VCC | | | |
| P150 | PWR | VDD_IN | _VCC | | | |
| P151 | PWR | VDD_IN | _VCC | | | |
| P152 | PWR | VDD_IN | _VCC | | | |
| P153 | PWR | VDD_IN | _VCC | | | |
| P154 | PWR | VDD_IN | _VCC | | | |
| P155 | PWR | VDD_IN | _VCC | | | |
| P156 | PWR | VDD_IN | _VCC | | | |

Table 10: X1 pin assignment – bottom side – Secondary pins Primary pins – Alternate functions

| MXM3 Pins | Signal Group | SMARC Signal | Soc Signal | Soc Ball Name | Power Group | Note |
|---|---|---|---|---|---|---|
| S1 | CSI | CSI1_TX+ / I2C_CAM1_CK | SPDIF_TX | AE18 | NVCC_SAI2_SAI3_SPDIF | |
| S2 | CSI | CSI1_TX- / I2C_CAM1_DAT | SPDIF_RX | AD18 | NVCC_SAI2_SAI3_SPDIF | |
| S3 | CSI | GND | _GND | | | |
| S4 | CSI | RSVD | | Not Connected | | |
| S5 | CSI | CSI0_TX+ / I2C_CAM0_CK | I2C3_SCL | AJ7 | NVCC_I2C_UART | |
| S6 | CSI | CAM_MCK | GPIO1_IO15 | B5 | NVCC_GPIO1 | |
| S7 | CSI | CSI0_TX- / I2C_CAM0_DAT | I2C3_SDA | AJ6 | NVCC_I2C_UART | |
| S8 | CSI | CSI0_CK+ | MIPI_CSI2_CLK_P | A23 | MIPI_VREG1_CAP | |
| S9 | CSI | CSI0_CK- | MIPI_CSI2_CLK_N | B23 | MIPI_VREG1_CAP | |
| S10 | CSI | GND | _GND | | | |
| S11 | CSI | CSI0_RX0+ | MIPI_CSI2_D0_P | A25 | MIPI_VREG1_CAP | |
| S12 | CSI | CSI0_RX0- | MIPI_CSI2_D0_N | B25 | MIPI_VREG1_CAP | |
| S13 | CSI | GND | _GND | | | |
| S14 | CSI | CSI0_RX1+ | MIPI_CSI2_D1_P | A24 | MIPI_VREG1_CAP | |
| S15 | CSI | CSI0_RX1- | MIPI_CSI2_D1_N | B24 | MIPI_VREG1_CAP | |
| S16 | CSI | GND | _GND | | | |
| S17 | Ethernet | GBE1_MDI0+ | ETH_1 PHY | | | |
| S18 | Ethernet | GBE1_MDI0- | ETH_1 PHY | | | |
| S19 | Ethernet | GBE1_LINK_MID# | ETH_1 PHY | | | Level Shifted - MOSFET - Output - OD |
| S20 | Ethernet | GBE1_MDI1+ | ETH_1 PHY | | | |
| S21 | Ethernet | GBE1_MDI1- | ETH_1 PHY | | | |
| S22 | Ethernet | GBE1_LINK_MAX# | ETH_1 PHY | | | Level Shifted - MOSFET - Output - OD |
| S23 | Ethernet | GBE1_MDI2+ | ETH_1 PHY | | | |

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Table 10: X1 pin assignment – bottom side – Secondary pins Primary pins – Alternate functions (Continued)

| MXM3 Pins | Signal Group | SMARC Signal | Soc Signal | Soc Ball Name | Power Group | Note |
|---|---|---|---|---|---|---|
| S24 | Ethernet | GBE1_MDI2- | ETH_1 PHY | | | |
| S25 | Ethernet | GND | _GND | | | |
| S26 | Ethernet | GBE1_MDI3+ | ETH_1 PHY | | | |
| S27 | Ethernet | GBE1_MDI3- | ETH_1 PHY | | | |
| S28 | Ethernet | GBE1_CTREF | | Not Connected | | |
| S29 | PCIe/ETH SERDES | PCIE_D_TX+ / SERDES_0_TX+ | | Not Connected | | |
| S30 | PCIe/ETH SERDES | PCIE_D_TX- / SERDES_0_TX- | | Not Connected | | |
| S31 | PCIe/ETH SERDES | GBE1_LINK_ACT# | ETH_1 PHY | | | Level Shifted - MOSFET - Output - OD |
| S32 | PCIe/ETH SERDES | PCIE_D_RX+ / SERDES_0_RX+ | | Not Connected | | |
| S33 | PCIe/ETH SERDES | PCIE_D_RX- / SERDES_0_RX- | | Not Connected | | |
| S34 | USB | GND | _GND | | | |
| S35 | USB | USB4+ | USB_Hub | | | |
| S36 | USB | USB4- | USB_Hub | | | |
| S37 | USB | USB3_VBUS_DET | | Not Connected | | 5V Capable |
| S38 | I2S | AUDIO_MCK | SAI1_MCLK | AE12 | NVCC_SAI1_SAI5 | |
| S39 | I2S | I2S0_LRCK | SAI5_RXD1 | AD16 | NVCC_SAI1_SAI5 | |
| S40 | I2S | I2S0_SDOUT | SAI5_RXFS | AC14 | NVCC_SAI1_SAI5 | |
| S41 | I2S | I2S0_SDIN | SAI1_RXD0 | AC10 | NVCC_SAI1_SAI5 | |
| S42 | I2S | I2S0_CK | SAI5_MCLK | AF14 | NVCC_SAI1_SAI5 | |
| S43 | QSPI | ESPI_ALERT0# | | Not Connected | | |
| S44 | QSPI | ESPI_ALERT1# | | Not Connected | | |
| S45 | ETH SERDES | MDIO_CLK | | Not Connected | | |
| S46 | ETH SERDES | MDIO_DAT | | Not Connected | | |

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Table 10: X1 pin assignment – bottom side – Secondary pins Primary pins – Alternate functions (Continued)

| MXM3 Pins | Signal Group | SMARC Signal | Soc Signal | Soc Ball Name | Power Group | Note |
|---|---|---|---|---|---|---|
| S47 | I2C | GND | _GND | | | |
| S48 | I2C | I2C_GP_CK | I2C4_SCL | AF8 | NVCC_I2C_UART | |
| S49 | I2C | I2C_GP_DAT | I2C4_SDA | AD8 | NVCC_I2C_UART | |
| S50 | HDA | HDA_SYNC / I2S2_LRCK | SAI3_TXFS | AC16 | NVCC_SAI2_SAI3_SPDIF | |
| S51 | HDA | HDA_SDO / I2S2_SDOUT | SAI3_TXD | AH18 | NVCC_SAI2_SAI3_SPDIF | |
| S52 | HDA | HDA_SDI / I2S2_SDIN | SAI3_RXD | AF18 | NVCC_SAI2_SAI3_SPDIF | |
| S53 | HDA | HDA_CK / I2S2_CK | SAI3_TXC | AH19 | NVCC_SAI2_SAI3_SPDIF | |
| S54 | CTRL | SATA_ACT# | | Not Connected | | |
| S55 | CTRL | USB5_EN_OC# | | Not Connected | | |
| S56 | QSPI | ESPI_IO_2 / QSPI_IO_2 | | Not Connected | | |
| S57 | QSPI | ESPI_IO_3 / QSPI_IO_3 | | Not Connected | | |
| S58 | QSPI | ESPI_RESET# | | Not Connected | | |
| S59 | USB | USB5+ | | Not Connected | | |
| S60 | USB | USB5- | | Not Connected | | |
| S61 | USB | GND | _GND | | | |
| S62 | USB | USB3_SSTX+ | USB_Hub | | | |
| S63 | USB | USB3_SSTX- | USB_Hub | | | |
| S64 | USB | GND | _GND | | | |
| S65 | USB | USB3_SSRX+ | USB_Hub | | | |
| S66 | USB | USB3_SSRX- | USB_Hub | | | |
| S67 | USB | GND | _GND | | | |
| S68 | USB | USB3+ | USB_Hub | | | |
| S69 | USB | USB3- | USB_Hub | | | |

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Table 10: X1 pin assignment – bottom side – Secondary pins Primary pins – Alternate functions (Continued)

| MXM3 Pins | Signal Group | SMARC Signal | Soc Signal | Soc Ball Name | Power Group | Note |
|---|---|---|---|---|---|---|
| S70 | USB | GND | _GND | | | |
| S71 | USB | USB2_SSTX+ | USB_Hub | | | |
| S72 | USB | USB2_SSTX- | USB_Hub | | | |
| S73 | USB | GND | _GND | | | |
| S74 | USB | USB2_SSRX+ | USB_Hub | | | |
| S75 | USB | USB2_SSRX- | USB_Hub | | | |
| S76 | PCIe | PCIE_B_RST# | | Not Connected | | |
| key | | | | | | |
| key | | | | | | |
| key | | | | | | |
| S77 | PCIe | PCIE_C_RST# | | Not Connected | | |
| S78 | PCIe | PCIE_C_RX+ / SERDES_1_RX+ | | Not Connected | | |
| S79 | PCIe | PCIE_C_RX- / SERDES_1_RX- | | Not Connected | | |
| S80 | PCIe | GND | _GND | | | |
| S81 | PCIe | PCIE_C_TX+ / SERDES_1_TX+ | | Not Connected | | |
| S82 | PCIe | PCIE_C_TX- / SERDES_1_TX- | | Not Connected | | |
| S83 | PCIe | GND | _GND | | | |
| S84 | PCIe | PCIE_B_REFCK+ | | Not Connected | | |
| S85 | PCIe | PCIE_B_REFCK- | | Not Connected | | |
| S86 | PCIe | GND | _GND | | | |
| S87 | PCIe | PCIE_B_RX+ | | Not Connected | | |
| S88 | PCIe | PCIE_B_RX- | | Not Connected | | |
| S89 | PCIe | GND | _GND | | | |

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Table 10: X1 pin assignment – bottom side – Secondary pins Primary pins – Alternate functions (Continued)

| MXM3 Pins | Signal Group | SMARC Signal | Soc Signal | Soc Ball Name | Power Group | Note |
|---|---|---|---|---|---|---|
| S90 | PCIe | PCIE_B_TX+ | | Not Connected | | |
| S91 | PCIe | PCIE_B_TX- | | Not Connected | | |
| S92 | PCIe | GND | _GND | | | |
| S93 | Display Port | DP0_LANE0+ | | Not Connected | | |
| S94 | Display Port | DP0_LANE0- | | Not Connected | | |
| S95 | Display Port | DP0_AUX_SEL | | Not Connected | | |
| S96 | Display Port | DP0_LANE1+ | | Not Connected | | |
| S97 | Display Port | DP0_LANE1- | | Not Connected | | |
| S98 | Display Port | DP0_HPD | | Not Connected | | |
| S99 | Display Port | DP0_LANE2+ | | Not Connected | | |
| S100 | Display Port | DP0_LANE2- | | Not Connected | | |
| S101 | Display Port | GND | _GND | | | |
| S102 | Display Port | DP0_LANE3+ | | Not Connected | | |
| S103 | Display Port | DP0_LANE3- | | Not Connected | | |
| S104 | Display Port | USB3_OTG_ID | | Not Connected | | |
| S105 | Display Port | DP0_AUX+ | | Not Connected | | |
| S106 | Display Port | DP0_AUX- | | Not Connected | | |
| S107 | LVDS | LCD1_BKLT_EN | GPIO_Expander | | | |
| S108 | LVDS | LVDS1_CK+ / eDP1_AUX+ / DSI1_CLK+ | LVDS1_CLK_P | A28 | VDD_LVDS_1P8 | Alternate Function: MIPI_DSI1_CLK_P |
| S109 | LVDS | LVDS1_CK- / eDP1_AUX- / DSI1_CLK- | LVDS1_CLK_N | B28 | VDD_LVDS_1P8 | Alternate Function: MIPI_DSI1_CLK_N |
| S110 | LVDS | GND | _GND | | | |
| S111 | LVDS | LVDS1_0+ / eDP1_TX0+ / DSI1_D0+ | LVDS1_D0_P | A26 | VDD_LVDS_1P8 | Alternate Function: MIPI_DSI1_D0_P |
| S112 | LVDS | LVDS1_0- / eDP1_TX0- / DSI1_D0- | LVDS1_D0_N | B26 | VDD_LVDS_1P8 | Alternate Function: MIPI_DSI1_D0_N |

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Table 10: X1 pin assignment – bottom side – Secondary pins Primary pins – Alternate functions (Continued)

| MXM3 Pins | Signal Group | SMARC Signal | Soc Signal | Soc Ball Name | Power Group | Note |
|---|---|---|---|---|---|---|
| S113 | LVDS | eDP1_HPD / DSI1_TE | | Not Connected | | |
| S114 | LVDS | LVDS1_1+ / eDP1_TX1+ / DSI1_D1+ | LVDS1_D1_P | A27 | VDD_LVDS_1P8 | Alternate Function: MIPI_DSI1_D1_P |
| S115 | LVDS | LVDS1_1- / eDP1_TX1- / DSI1_D1- | LVDS1_D1_N | B27 | VDD_LVDS_1P8 | Alternate Function: MIPI_DSI1_D1_N |
| S116 | LVDS | LCD1_VDD_EN | GPIO_Expander | | | |
| S117 | LVDS | LVDS1_2+ / eDP1_TX2+ / DSI1_D2+ | LVDS1_D2_P | B29 | VDD_LVDS_1P8 | Alternate Function: MIPI_DSI1_D2_P |
| S118 | LVDS | LVDS1_2- / eDP1_TX2- / DSI1_D2- | LVDS1_D2_N | C28 | VDD_LVDS_1P8 | Alternate Function: MIPI_DSI1_D2_N |
| S119 | LVDS | GND | _GND | | | |
| S120 | LVDS | LVDS1_3+ / eDP1_TX3+ / DSI1_D3+ | LVDS1_D3_P | C29 | VDD_LVDS_1P8 | Alternate Function: MIPI_DSI1_D3_P |
| S121 | LVDS | LVDS1_3- / eDP1_TX3- / DSI1_D3- | LVDS1_D3_N | D28 | VDD_LVDS_1P8 | Alternate Function: MIPI_DSI1_D3_N |
| S122 | LVDS | LCD1_BKLT_PWM | SPDIF_EXT_CLK | AC18 | NVCC_SAI2_SAI3_SPDIF | |
| S123 | LVDS | GPIO13 | GPIO1_IO13 | A6 | NVCC_GPIO1 | |
| S124 | LVDS | GND | _GND | | | |
| S125 | LVDS | LVDS0_0+ / eDP0_TX0+ / DSI0_D0+ | LVDS0_D0_P | D29 | VDD_LVDS_1P8 | |
| S126 | LVDS | LVDS0_0- / eDP0_TX0- / DSI0_D0- | LVDS0_D0_N | E28 | VDD_LVDS_1P8 | |
| S127 | LVDS | LCD0_BKLT_EN | GPIO_Expander | | | |
| S128 | LVDS | LVDS0_1+ / eDP0_TX1+ / DSI0_D1+ | LVDS0_D1_P | E29 | VDD_LVDS_1P8 | |
| S129 | LVDS | LVDS0_1- / eDP0_TX1- / DSI0_D1- | LVDS0_D1_N | F28 | VDD_LVDS_1P8 | |
| S130 | LVDS | GND | _GND | | | |
| S131 | LVDS | LVDS0_2+ / eDP0_TX2+ / DSI0_D2+ | LVDS0_D2_P | G29 | VDD_LVDS_1P8 | |
| S132 | LVDS | LVDS0_2- / eDP0_TX2- / DSI0_D2- | LVDS0_D2_N | H28 | VDD_LVDS_1P8 | |
| S133 | LVDS | LCD0_VDD_EN | GPIO_Expander | | | |
| S134 | LVDS | LVDS0_CK+ / eDP0_AUX+ / DSI0_CLK+ | LVDS0_CLK_P | F29 | VDD_LVDS_1P8 | |
| S135 | LVDS | LVDS0_CK- / eDP0_AUX- / DSI0_CLK- | LVDS0_CLK_N | G28 | VDD_LVDS_1P8 | |

*Continued on next page*

Table 10: X1 pin assignment – bottom side – Secondary pins Primary pins – Alternate functions (Continued)

| MXM3 Pins | Signal Group | SMARC Signal | Soc Signal | Soc Ball Name | Power Group | Note |
|---|---|---|---|---|---|---|
| S136 | LVDS | GND | _GND | | | |
| S137 | LVDS | LVDS0_3+ / eDP0_TX3+ / DSI0_D3+ | LVDS0_D3_P | H29 | VDD_LVDS_1P8 | |
| S138 | LVDS | LVDS0_3- / eDP0_TX3- / DSI0_D3- | LVDS0_D3_N | J28 | VDD_LVDS_1P8 | |
| S139 | LVDS | I2C_LCD_CK | I2C2_SCL | AH6 | NVCC_I2C_UART | |
| S140 | LVDS | I2C_LCD_DAT | I2C2_SDA | AE8 | NVCC_I2C_UART | |
| S141 | CTRL | LCD0_BKLT_PWM | GPIO1_IO11 | D8 | NVCC_GPIO1 | |
| S142 | CTRL | GPIO12 | GPIO1_IO08 | A8 | NVCC_GPIO1 | |
| S143 | CTRL | GND | _GND | | | |
| S144 | CTRL | eDP0_HPD / DSI0_TE | | Not Connected | | |
| S145 | CTRL | WDT_TIME_OUT# | MCU | | | |
| S146 | CTRL | PCIE_WAKE# | SAI1_RXFS | AJ9 | NVCC_SAI1_SAI5 | Level Shifted - Diode - Input - OD, CMOS - 10k PU |
| S147 | CTRL | VDD_RTC | | | | |
| S148 | CTRL | LID# | MCU | | | |
| S149 | CTRL | SLEEP# | NAND_CE0_B | L26 | NVCC_NAND | |
| S150 | CTRL | VIN_PWR_BAD# | MCU | | | 5V Capable |
| S151 | CTRL | CHARGING# | MCU | | | |
| S152 | CTRL | CHARGER_PRSNT# | MCU | | | |
| S153 | CTRL | CARRIER_STBY# | MCU | | | |
| S154 | CTRL | CARRIER_PWR_ON | MCU | | | |
| S155 | CTRL | FORCE_RECOV# | MCU | | | |
| S156 | CTRL | BATLOW# | MCU | | | |
| S157 | CTRL | TEST# | MCU | | | |

# 9 I/O Pins

## 9.1 Function Multiplexing

Low-speed I/O pins of the NXP i.MX 8M Plus SoC can be configured for any of the (and up to) seven alternate functions. Most of the pins can also be used as GPIOs (General-Purpose I/O, sometimes also referred to as Digital I/O). For example, the i.MX 8M Plus signal pin on the **SMARC MXM3 pin P129** has the primary function **UART1_TX**. Besides this UART function, the pin can also be configured as **ECSPI3_MOSI** (SPI master out, slave in) and **GPIO5_IO23** (GPIO).

The default setting for this pin is the primary function **UART1_TX**. The SMARC standard defines (Section 4.7) that some pins shall have a specific function. It is strongly recommended, whenever possible, to use a function that is compatible with the SMARC specification. This guarantees the best compatibility with the standard software and with other modules.

Some of the alternate functions are available on more than one pin. Care should be taken to ensure that two pins are not configured with the same function. This could lead to system instability and undefined behavior.

On Table 14 on page 36 there is a list of all pins which have alternate functions. There you can find which alternate functions are available for each individual pin.

## 9.2 Pin Control

The alternate function of each pin can be changed independently. Every pin has a Pad Mux Register in which the following settings can be configured (some settings might not be available for certain pins). The register is called IOMUXC_SW_MUX_CTL_PAD_x, where x is the name of the i.MX 8M Plus pin. More information about the available register settings can be found in the i.MX 8M Plus Reference Manual.

Table 11: Pad Mux Register

| Bit | Field | Description | Remarks |
|---|---|---|---|
| 31-5 | Reserved | | |
| 4 | SION | 0 Software Input On Field disabled<br>1 Software Input On Field enable | Force the selected mux mode input path |
| 3 | Reserved | | |
| 2-0 | MUX_MODE | 000 Select mux mode: ALT0 mux port<br>001 Select mux mode: ALT1 mux port<br>010 Select mux mode: ALT2 mux port<br>011 Select mux mode: ALT3 mux port<br>100 Select mux mode: ALT4 mux port<br>101 Select mux mode: ALT5 mux port (GPIO)<br>110 Select mux mode: ALT6 mux port | Check section 4.4 for the available alternate function of the pin |

For most pins, the ALT5 multiplexing option is reserved for the GPIO function. However, there are a few pins that feature the GPIO function on ALT0. Carefully check Table 14 on page 36 and the reference manual provided by NXP.

The pins have an additional register that allows the configuration of pull-up/down resistors, drive strength, and other settings. The register is called IOMUXC_SW_PAD_CTL_PAD_x, where x is the name of the i.MX 8M Plus pin. Some settings might not be available on certain pins. More information about the available register settings can be found in the i.MX 8M Plus Reference Manual.

Table 12: Pad Mux Register

| Bit | Field | Description | Remarks |
|---|---|---|---|
| 31-9 | Reserved | | |
| 8 | PE | 0 Pull resistor disabled<br>1 Pull resistor enable | |
| 7 | HYS | 0 CMOS input<br>1 Schmitt trigger input | |
| 6 | PUE | 0 Select pull-down resistor<br>1 Select pull-up resistor | Typical pull-up value 22kΩ<br>Typical pull-down value 23kΩ |
| 5 | ODE | 0 Output is CMOS<br>1 Output is open-drain | |
| 4-3 | FSE | 0x Slow Slew Rate<br>1x Fast Slew Rate | Use a slow slew rate, if possible, for reducing EMC problems |
| 2-0 | MUX_MODE | 00x Drive strength X1<br>01x Drive strength X2<br>10x Drive strength X4<br>11x Drive strength X6 | If possible, decrease the drive strength to reduce EMC problems |

Input functions that are available at more than one physical pin require an additional input multiplexer. This multiplexer is configured by a register called IOMUXC_x_SELECT_INPUT, where x is the name of the input function. More information about this register can be found in the i.MX 8M Plus Reference Manual.

## 9.3 SoC Functions List

Table 14 on page 36 shows a list of all the i.MX 8M Plus pins that are available on the MXM3 connector. It shows the alternate functions that are available for each pin. For most of the pins, the GPIO functionality is defined as the ALT5 function.

Table 13: Function Short Forms

| Short Form | Description |
|---|---|
| ADC | Analog to Digital Converter input |
| CAAM | Cryptographic Acceleration and Assurance Module |
| CAN | Controller Area Network |
| CCM | Clock Control Module |
| CSI | Camera Serial Interface |
| CSU | Central Security Unit |
| EARC | Enhanced Audio Return Channel (for HDMI) |
| ECC | Error-Correcting Code |
| ECSPI | Enhanced Configurable SPI |
| ENET | Ethernet MAC interface |
| GPIO | General-Purpose Input Output |
| GPC | General Power Controller |
| GPT | General Purpose Timer |
| HDMI | High-Definition Multimedia Interface |
| I2C | Inter-Integrated Circuit |
| ISP | Image Signal Processor |

*Continued on next page*

Table 13: Function Short Forms (Continued)

| Short Form | Description |
|---|---|
| JTAG | Test Interface |
| LVDS | FPD-Link/FlatLink Display interface |
| MIPI_CSI | MIPI CSI Subsystem |
| MIPI_DSI | MIPI DSI Subsystem |
| NAND | Interface for NAND Flash |
| NPU | Neural Processing Unit |
| PCIE | PCI Express |
| PDM | Pulse-Density Modulation Microphone Input |
| PWM | Pulse Width Modulation output |
| QSPI | Quad Serial Peripheral Interface |
| SAI | Serial Interface for Audio (I2S and AC97) |
| SDMA | Smart Direct Memory Access Controller |
| SNVS | Secure Non-Volatile Storage |
| SPDIF | Sony/Philips Digital Interface |
| UART | Universal Asynchronous Receiver/Transmitter |
| USB | Universal Serial Bus |
| USDHC | Ultra-Secured Digital Host Controller (interface for SD and MMC cards) |
| VPU | Video Processing Unit (acceleration for video encoding and decoding) |

### 9.3.1 Alternate Functions

Table 14: X1 pin Alternate Functions Primary pins – Secondary pins

| MXM3 Pin | SMARC Signal | Soc Signal | Soc Ball Name | ALT0 | ALT1 | ALT2 | ALT3 | ALT4 | ALT5 | ALT6 |
|---|---|---|---|---|---|---|---|---|---|---|
| P1 | SMB_ALERT# | NAND_READY_B | T28 | NAND_READY_B | | USDHC3_RESET_B | | I2C3_SCL | GPIO3_IO16 | |
| P3 | CSI1_CK+ | MIPI_CSI1_CLK_P | D22 | MIPI_CSI1_CLK_P | | | | | | |
| P4 | CSI1_CK- | MIPI_CSI1_CLK_N | E22 | MIPI_CSI1_CLK_N | | | | | | |
| P5 | GBE1_SDP | SAI1_RXC | AH8 | SAI1_RX_BCLK | SAI5_RX_BCLK | | PDM_CLK | ENET1_1588_EVENT0_OUT | GPIO4_IO1 | |
| P6 | GBE0_SDP | GPIO1_IO09 | B8 | GPIO1_IO9 | ENET_QOS_1588_EVENT0_OUT | PWM2_OUT | ISP_SHUTTER_OPEN_1 | USDHC3_RESET_B | SDMA2_EXT_EVENT0 | |
| P7 | CSI1_RX0+ | MIPI_CSI1_D0_P | D18 | MIPI_CSI1_D0_P | | | | | | |
| P8 | CSI1_RX0- | MIPI_CSI1_D0_N | E18 | MIPI_CSI1_D0_N | | | | | | |
| P10 | CSI1_RX1+ | MIPI_CSI1_D1_P | D20 | MIPI_CSI1_D1_P | | | | | | |
| P11 | CSI1_RX1- | MIPI_CSI1_D1_N | E20 | MIPI_CSI1_D1_N | | | | | | |
| P13 | CSI1_RX2+ | MIPI_CSI1_D2_P | D24 | MIPI_CSI1_D2_P | | | | | | |
| P14 | CSI1_RX2- | MIPI_CSI1_D2_N | E24 | MIPI_CSI1_D2_N | | | | | | |
| P16 | CSI1_RX3+ | MIPI_CSI1_D3_P | D26 | MIPI_CSI1_D3_P | | | | | | |
| P17 | CSI1_RX3- | MIPI_CSI1_D3_N | E26 | MIPI_CSI1_D3_N | | | | | | |
| P31 | SPI0_CS1# | SAI3_RXFS | AJ19 | SAI3_RX_SYNC | SAI2_RX_DATA1 | SAI5_RX_SYNC | SAI3_RX_DATA1 | SPDIF1_IN | GPIO4_IO28 | PDM_BIT_STREAM0 |
| P33 | SDIO_WP | SD2_WP | AC26 | USDHC2_WP | | | | | GPIO2_IO20 | CORESIGHT_EVENTI |
| P34 | SDIO_CMD | SD2_CMD | AB28 | USDHC2_CMD | | ECSPI2_MOSI | UART4_TX | PDM_CLK | GPIO2_IO14 | |
| P35 | SDIO_CD# | SD2_CD_B | AD29 | USDHC2_CD_B | | | | | GPIO2_IO12 | |
| P36 | SDIO_CK | SD2_CLK | AB29 | USDHC2_CLK | | ECSPI2_SCLK | UART4_RX | | GPIO2_IO13 | |
| P37 | SDIO_PWR_EN | SD2_RESET_B | AD28 | USDHC2_RESET_B | | | | | GPIO2_IO19 | SRC_SYSTEM_RESET |
| P39 | SDIO_D0 | SD2_DATA0 | AC28 | USDHC2_DATA0 | | I2C4_SDA | UART2_RX | PDM_BIT_STREAM0 | GPIO2_IO15 | |
| P40 | SDIO_D1 | SD2_DATA1 | AC29 | USDHC2_DATA1 | | I2C4_SCL | UART2_TX | PDM_BIT_STREAM1 | GPIO2_IO16 | |
| P41 | SDIO_D2 | SD2_DATA2 | AA26 | USDHC2_DATA2 | | ECSPI2_SS0 | SPDIF1_OUT | PDM_BIT_STREAM2 | GPIO2_IO17 | |

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Table 14: X1 pin Alternate Functions Primary pins – Secondary pins (Continued)

| MXM3 Pin | SMARC Signal | Soc Signal | Soc Ball Name | ALT0 | ALT1 | ALT2 | ALT3 | ALT4 | ALT5 | ALT6 |
|---|---|---|---|---|---|---|---|---|---|---|
| P42 | SDIO_D3 | SD2_DATA3 | AA25 | USDHC2_DATA3 | | ECSPI2_MISO | SPDIF1_IN | PDM_BIT_STREAM3 | GPIO2_IO18 | SRC_EARLY_RESET |
| P43 | SPI0_CS0# | ECSPI1_SS0 | AE20 | ECSPI1_SS0 | UART3_RTS_B | I2C2_SDA | SAI7_TX_SYNC | | GPIO5_IO9 | |
| P44 | SPI0_CK | ECSPI1_SCLK | AF20 | ECSPI1_SCLK | UART3_RX | I2C1_SCL | SAI7_RX_SYNC | | GPIO5_IO6 | |
| P45 | SPI0_DIN | ECSPI1_MISO | AD20 | ECSPI1_MISO | UART3_CTS_B | I2C2_SCL | SAI7_RX_DATA0 | | GPIO5_IO8 | |
| P46 | SPI0_DO | ECSPI1_MOSI | AC20 | ECSPI1_MOSI | UART3_TX | I2C1_SDA | SAI7_RX_BCLK | | GPIO5_IO7 | |
| P54 | ESPI_CS0# / SPI1_CS0# / QSPI_CS0# | ECSPI2_SS0 | AJ22 | ECSPI2_SS0 | UART4_RTS_B | I2C4_SDA | | CCM_CLKO2 | GPIO5_IO13 | |
| P55 | ESPI_CS1# / SPI1_CS1# / QSPI_CS1# | SAI1_RXD1 | AF10 | SAI1_RX_DATA1 | SAI5_RX_DATA1 | | PDM_BIT_STREAM1 | ENET1_1588_EVENT1_OUT | GPIO4_IO3 | |
| P56 | ESPI_CK / SPI1_CK / QSPI_CK | ECSPI2_SCLK | AH21 | ECSPI2_SCLK | UART4_RX | I2C3_SCL | SAI7_TX_BCLK | | GPIO5_IO10 | |
| P57 | ESPI_IO_1 / SPI1_DIN / QSPI_IO_1 | ECSPI2_MISO | AH20 | ECSPI2_MISO | UART4_CTS_B | I2C4_SCL | SAI7_MCLK | CCM_CLKO1 | GPIO5_IO12 | |
| P58 | ESPI_IO_0 / SPI1_DO / QSPI_IO_0 | ECSPI2_MOSI | AJ21 | ECSPI2_MOSI | UART4_TX | I2C3_SDA | SAI7_TX_DATA0 | | GPIO5_IO11 | |
| P60 | USB0+ | USB1_D_P | D10 | USB1_D_P | | | | | | |
| P61 | USB0- | USB1_D_N | E10 | USB1_D_N | | | | | | |
| P62 | USB0_EN_OC# | GPIO1_IO12 | A5 | GPIO1_IO12 | USB1_OTG_PWR | | | | SDMA2_EXT_EVENT1 | |
| P63 | USB0_VBUS_DET | USB1_VBUS | A11 | USB1_VBUS | | | | | | |
| P64 | USB0_OTG_ID | SAI3_MCLK | AJ20 | SAI3_MCLK | PWM4_OUT | SAI5_MCLK | | SPDIF1_OUT | GPIO5_IO2 | SPDIF1_IN |
| P75 | PCIE_A_RST# | SAI1_TXD7 | AJ13 | SAI1_TX_DATA7 | SAI6_MCLK | | PDM_CLK | ENET1_TX_ER | GPIO4_IO19 | |
| P78 | PCIE_A_CKREQ# | NAND_DQS | R26 | NAND_DQS | QSPI_A_DQS | SAI3_MCLK | ISP_SHUTTER_OPEN_0 | I2C3_SCL | GPIO3_IO14 | |
| P83 | PCIE_A_REFCK+ | PCIE_REF_PAD _CLK_P | D16 | PCIE1_REF_PAD _CLK_P | | | | | | |

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Table 14: X1 pin Alternate Functions Primary pins – Secondary pins (Continued)

| MXM3 Pin | SMARC Signal | Soc Signal | Soc Ball Name | ALT0 | ALT1 | ALT2 | ALT3 | ALT4 | ALT5 | ALT6 |
|---|---|---|---|---|---|---|---|---|---|---|
| P84 | PCIE_A_REFCK- | PCIE_REF_PAD _CLK_N | E16 | PCIE1_REF_PAD _CLK_N | | | | | | |
| P86 | PCIE_A_RX+ | PCIE_RXN_P | A14 | PCIE1_RXN_P | | | | | | |
| P87 | PCIE_A_RX- | PCIE_RXN_N | B14 | PCIE1_RXN_N | | | | | | |
| P89 | PCIE_A_TX+ | PCIE_TXN_P | A15 | PCIE1_TXN_P | | | | | | |
| P90 | PCIE_A_TX- | PCIE_TXN_N | B15 | PCIE1_TXN_N | | | | | | |
| P104 | HDMI_HPD / DP1_HPD | HDMI_HPD | AE22 | HDMI_HPD | HDMI_HPD_O | | I2C6_SDA | CAN2_RX | GPIO3_IO29 | |
| P105 | HDMI_CTRL_CK / DP1_AUX+ | HDMI_DDC_SCL | AC22 | HDMI_SCL | | | I2C5_SCL | CAN1_TX | GPIO3_IO26 | |
| P106 | HDMI_CTRL_DAT / DP1_AUX- | HDMI_DDC_SDA | AF22 | HDMI_SDA | | | I2C5_SDA | CAN1_RX | GPIO3_IO27 | |
| P108 | GPIO0 / CAM0_PWR# | GPIO_Expander | | GPIO1_IO0 | CCM_ENET_PHY _REF_CLK_ROOT | | ISP_FL_TRIG_0 | | CCM_REF_CLK_32K | CCM_EXT_CLK1 |
| P109 | GPIO1 / CAM1_PWR# | GPIO_Expander | | GPIO1_IO1 | PWM1_OUT | | ISP_SHUTTER_TRIG_0 | | CCM_REF_CLK_24M | CCM_EXT_CLK2 |
| P110 | GPIO2 / CAM0_RST# | GPIO_Expander | | GPIO1_IO5 | M7_NMI | | ISP_FL_TRIG_1 | | CCM_PMIC_READY | |
| P111 | GPIO3 / CAM1_RST# | GPIO_Expander | | GPIO1_IO6 | ENET_QOS_MDC | | ISP_SHUTTER_TRIG_1 | | USDHC1_CD_B | CCM_EXT_CLK3 |
| P112 | GPIO4 / HDA_RST# | SAI1_TXD6 | AC12 | SAI1_TX_DATA6 | SAI6_RX_SYNC | SAI6_TX_SYNC | | ENET1_RX_ER | GPIO4_IO18 | |
| P113 | GPIO5 / PWM_OUT | GPIO1_IO10 | B7 | GPIO1_IO10 | USB1_OTG_ID | PWM3_OUT | | | | |
| P114 | GPIO6 / TACHIN | SAI3_RXC | AJ18 | SAI3_RX_BCLK | SAI2_RX_DATA2 | SAI5_RX_BCLK | GPT1_CLK | UART2_CTS_B | GPIO4_IO29 | PDM_CLK |
| P115 | GPIO7 | GPIO1_IO00 | A7 | GPIO1_IO0 | CCM_ENET_PHY _REF_CLK_ROOT | | ISP_FL_TRIG_0 | | CCM_REF_CLK_32K | CCM_EXT_CLK1 |
| P116 | GPIO8 | GPIO1_IO01 | E8 | GPIO1_IO1 | PWM1_OUT | | ISP_SHUTTER_TRIG_0 | | CCM_REF_CLK_24M | CCM_EXT_CLK2 |

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Table 14: X1 pin Alternate Functions Primary pins – Secondary pins (Continued)

| MXM3 Pin | SMARC Signal | Soc Signal | Soc Ball Name | ALT0 | ALT1 | ALT2 | ALT3 | ALT4 | ALT5 | ALT6 |
|---|---|---|---|---|---|---|---|---|---|---|
| P117 | GPIO9 | GPIO1_IO05 | B4 | GPIO1_IO5 | M7_NMI | | ISP_FL_TRIG_1 | | CCM_PMIC_READY | |
| P118 | GPIO10 | GPIO1_IO06 | A3 | GPIO1_IO6 | ENET_QOS_MDC | | ISP_SHUTTER_TRIG_1 | | USDHC1_CD_B | CCM_EXT_CLK3 |
| P119 | GPIO11 | GPIO1_IO07 | F6 | GPIO1_IO7 | ENET_QOS_MDIO | | ISP_FLASH_TRIG_1 | | USDHC1_WP | CCM_EXT_CLK4 |
| P121 | I2C_PM_CK | HDMI_CEC | AD22 | HDMI_CEC | | | I2C6_SCL | CAN2_TX | GPIO3_IO28 | |
| P122 | I2C_PM_DAT | SAI5_RXC | AD14 | SAI5_RX_BCLK | SAI1_TX_DATA1 | PWM3_OUT | I2C6_SDA | PDM_CLK | GPIO3_IO20 | |
| P129 | SER0_TX | UART1_TXD | AJ3 | UART1_TX | ECSPI3_MOSI | | | | GPIO5_IO23 | |
| P130 | SER0_RX | UART1_RXD | AD6 | UART1_RX | ECSPI3_SCLK | | | | GPIO5_IO22 | |
| P131 | SER0_RTS# | SAI2_TXFS | AJ17 | SAI2_TX_SYNC | SAI5_TX_DATA1 | ENET_QOS_1588 _EVENT3_OUT | SAI2_TX_DATA1 | UART1_CTS_B | GPIO4_IO24 | PDM_BIT_STREAM2 |
| P132 | SER0_CTS# | SAI2_RXD0 | AJ14 | SAI2_RX_DATA0 | SAI5_TX_DATA0 | ENET_QOS_1588 _EVENT2_OUT | SAI2_TX_DATA1 | UART1_RTS_B | GPIO4_IO23 | PDM_BIT_STREAM3 |
| P134 | SER1_TX | UART4_TXD | AH5 | UART4_TX | UART2_RTS_B | | GPT1_CAPTURE1 | I2C6_SDA | GPIO5_IO29 | |
| P135 | SER1_RX | UART4_RXD | AJ5 | UART4_RX | UART2_CTS_B | PCIE1_CLKREQ_B | GPT1_COMPARE1 | I2C6_SCL | GPIO5_IO28 | |
| P136 | SER2_TX | UART2_TXD | AH4 | UART2_TX | ECSPI3_SS0 | | GPT1_COMPARE2 | | GPIO5_IO25 | |
| P137 | SER2_RX | UART2_RXD | AF6 | UART2_RX | ECSPI3_MISO | | GPT1_COMPARE3 | | GPIO5_IO24 | |
| P138 | SER2_RTS# | SD1_DATA5 | AA29 | USDHC1_DATA5 | ENET1_TX_ER | | I2C1_SDA | UART2_CTS_B | GPIO2_IO7 | |
| P139 | SER2_CTS# | SD1_DATA4 | U26 | USDHC1_DATA4 | ENET1_RGMII_TX_CTL | | I2C1_SCL | UART2_RTS_B | GPIO2_IO6 | |
| P140 | SER3_TX | UART3_TXD | AJ4 | UART3_TX | UART1_RTS_B | USDHC3_VSELECT | GPT1_CLK | CAN2_RX | GPIO5_IO27 | |
| P141 | SER3_RX | UART3_RXD | AE6 | UART3_RX | UART1_CTS_B | USDHC3_RESET_B | GPT1_CAPTURE2 | CAN2_TX | GPIO5_IO26 | |
| P143 | CAN0_TX | SAI2_TXD0 | AH16 | SAI2_TX_DATA0 | SAI5_TX_DATA3 | ENET_QOS_1588 _EVENT2_IN | CAN2_TX | ENET_QOS_1588 _EVENT2_AUX_IN | GPIO4_IO26 | SRC_BOOT_MODE4 |
| P144 | CAN0_RX | SAI2_MCLK | AJ15 | SAI2_MCLK | SAI5_MCLK | ENET_QOS_1588 _EVENT3_IN | CAN2_RX | ENET_QOS_1588 _EVENT3_AUX_IN | GPIO4_IO27 | SAI3_MCLK |
| P145 | CAN1_TX | SAI2_RXC | AJ16 | SAI2_RX_BCLK | SAI5_TX_BCLK | | CAN1_TX | UART1_RX | GPIO4_IO22 | PDM_BIT_STREAM1 |
| P146 | CAN1_RX | SAI2_TXC | AH15 | SAI2_TX_BCLK | SAI5_TX_DATA2 | | CAN1_RX | | GPIO4_IO25 | PDM_BIT_STREAM1 |

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Table 14: X1 pin Alternate Functions Primary pins – Secondary pins (Continued)

| MXM3 Pin | SMARC Signal | Soc Signal | Soc Ball Name | ALT0 | ALT1 | ALT2 | ALT3 | ALT4 | ALT5 | ALT6 |
|---|---|---|---|---|---|---|---|---|---|---|
| S1 | CSI1_TX+ / I2C_CAM1_CK | SPDIF_TX | AE18 | SPDIF1_OUT | PWM3_OUT | I2C5_SCL | GPT1_COMPARE1 | CAN1_TX | GPIO5_IO3 | |
| S2 | CSI1_TX- / I2C_CAM1_DAT | SPDIF_RX | AD18 | SPDIF1_IN | PWM2_OUT | I2C5_SDA | GPT1_COMPARE2 | CAN1_RX | GPIO5_IO4 | |
| S5 | CSI0_TX+ / I2C_CAM0_CK | I2C3_SCL | AJ7 | I2C3_SCL | PWM4_OUT | GPT2_CLK | ECSPI2_SCLK | | GPIO5_IO18 | |
| S6 | CAM_MCK | GPIO1_IO15 | B5 | GPIO1_IO15 | USB2_OTG_OC | | | USDHC3_WP | PWM4_OUT | CCM_CLKO2 |
| S7 | CSI0_TX- / I2C_CAM0_DAT | I2C3_SDA | AJ6 | I2C3_SDA | PWM3_OUT | GPT3_CLK | ECSPI2_MOSI | | GPIO5_IO19 | |
| S8 | CSI0_CK+ | MIPI_CSI2_CLK_P | A23 | MIPI_CSI2_CLK_P | | | | | | |
| S9 | CSI0_CK- | MIPI_CSI2_CLK_N | B23 | MIPI_CSI2_CLK_N | | | | | | |
| S11 | CSI0_RX0+ | MIPI_CSI2_D0_P | A25 | MIPI_CSI2_D0_P | | | | | | |
| S12 | CSI0_RX0- | MIPI_CSI2_D0_N | B25 | MIPI_CSI2_D0_N | | | | | | |
| S14 | CSI0_RX1+ | MIPI_CSI2_D1_P | A24 | MIPI_CSI2_D1_P | | | | | | |
| S15 | CSI0_RX1- | MIPI_CSI2_D1_N | B24 | MIPI_CSI2_D1_N | | | | | | |
| S38 | AUDIO_MCK | SAI1_MCLK | AE12 | SAI1_MCLK | SAI5_MCLK | SAI1_TX_BCLK | | ENET1_TX_CLK | GPIO4_IO20 | |
| S39 | I2S0_LRCK | SAI5_RXD1 | AD16 | SAI5_RX_DATA1 | SAI1_TX_DATA3 | SAI1_TX_SYNC | SAI5_TX_SYNC | PDM_BIT_STREAM1 | GPIO3_IO22 | CAN1_TX |
| S40 | I2S0_SDOUT | SAI5_RXFS | AC14 | SAI5_RX_SYNC | SAI1_TX_DATA0 | PWM4_OUT | I2C6_SCL | | GPIO3_IO19 | |
| S41 | I2S0_SDIN | SAI1_RXD0 | AC10 | SAI1_RX_DATA0 | SAI5_RX_DATA0 | SAI1_TX_DATA1 | PDM_BIT_STREAM0 | ENET1_1588_EVENT1_IN | GPIO4_IO2 | |
| S42 | I2S0_CK | SAI5_MCLK | AF14 | SAI5_MCLK | SAI1_TX_BCLK | PWM1_OUT | I2C5_SDA | | GPIO3_IO25 | CAN2_RX |
| S48 | I2C_GP_CK | I2C4_SCL | AF8 | I2C4_SCL | PWM2_OUT | PCIE1_CLKREQ_B | ECSPI2_MISO | | GPIO5_IO20 | |
| S49 | I2C_GP_DAT | I2C4_SDA | AD8 | I2C4_SDA | PWM1_OUT | | ECSPI2_SS0 | | GPIO5_IO21 | |
| S50 | HDA_SYNC / I2S2_LRCK | SAI3_TXFS | AC16 | SAI3_TX_SYNC | SAI2_TX_DATA1 | SAI5_RX_DATA1 | SAI3_TX_DATA1 | UART2_RX | GPIO4_IO31 | PDM_BIT_STREAM3 |
| S51 | HDA_SDO / I2S2_SDOUT | SAI3_TXD | AH18 | SAI3_TX_DATA0 | SAI2_TX_DATA3 | SAI5_RX_DATA3 | GPT1_CAPTURE2 | SPDIF1_EXT_CLK | GPIO5_IO1 | SRC_BOOT_MODE5 |

*Continued on next page*

Table 14: X1 pin Alternate Functions Primary pins – Secondary pins (Continued)

| MXM3 Pin | SMARC Signal | Soc Signal | Soc Ball Name | ALT0 | ALT1 | ALT2 | ALT3 | ALT4 | ALT5 | ALT6 |
|---|---|---|---|---|---|---|---|---|---|---|
| S52 | HDA_SDI / I2S2_SDIN | SAI3_RXD | AF18 | SAI3_RX_DATA0 | SAI2_RX_DATA3 | SAI5_RX_DATA0 | | UART2_RTS_B | GPIO4_IO30 | PDM_BIT_STREAM1 |
| S53 | HDA_CK / I2S2_CK | SAI3_TXC | AH19 | SAI3_TX_BCLK | SAI2_TX_DATA2 | SAI5_RX_DATA2 | GPT1_CAPTURE1 | UART2_TX | GPIO5_IO0 | PDM_BIT_STREAM2 |
| S62 | USB3_SSTX+ | USB2_TX_P | A13 | USB2_TX_P | | | | | | |
| S63 | USB3_SSTX- | USB2_TX_N | B13 | USB2_TX_N | | | | | | |
| S65 | USB3_SSRX+ | USB2_RX_P | A12 | USB2_RX_P | | | | | | |
| S66 | USB3_SSRX- | USB2_RX_N | B12 | USB2_RX_N | | | | | | |
| S71 | USB2_SSTX+ | USB1_TX_P | A10 | USB1_TX_P | | | | | | |
| S72 | USB2_SSTX- | USB1_TX_N | B10 | USB1_TX_N | | | | | | |
| S74 | USB2_SSRX+ | USB1_RX_P | A9 | USB1_RX_P | | | | | | |
| S75 | USB2_SSRX- | USB1_RX_N | B9 | USB1_RX_N | | | | | | |
| S107 | LCD1_BKLT_EN | SAI3_RXFS | AJ19 | SAI3_RX_SYNC | SAI2_RX_DATA1 | SAI5_RX_SYNC | SAI3_RX_DATA1 | SPDIF1_IN | GPIO4_IO28 | PDM_BIT_STREAM0 |
| S108 | LVDS1_CK+ / eDP1_AUX+ / DSI1_CLK+ | LVDS1_CLK_P | A28 | LVDS1_CLK_P | | | | | | |
| S109 | LVDS1_CK- / eDP1_AUX- / DSI1_CLK- | LVDS1_CLK_N | B28 | LVDS1_CLK_N | | | | | | |
| S111 | LVDS1_0+ / eDP1_TX0+ / DSI1_D0+ | LVDS1_D0_P | A26 | LVDS1_D0_P | | | | | | |
| S112 | LVDS1_0- / eDP1_TX0- / DSI1_D0- | LVDS1_D0_N | B26 | LVDS1_D0_N | | | | | | |
| S114 | LVDS1_1+ / eDP1_TX1+ / DSI1_D1+ | LVDS1_D1_P | A27 | LVDS1_D1_P | | | | | | |

*Continued on next page*

Table 14: X1 pin Alternate Functions Primary pins – Secondary pins (Continued)

| MXM3 Pin | SMARC Signal | Soc Signal | Soc Ball Name | ALT0 | ALT1 | ALT2 | ALT3 | ALT4 | ALT5 | ALT6 |
|---|---|---|---|---|---|---|---|---|---|---|
| S115 | LVDS1_1- / eDP1_TX1- / DSI1_D1- | LVDS1_D1_N | B27 | LVDS1_D1_N | | | | | | |
| S117 | LVDS1_2+ / eDP1_TX2+ / DSI1_D2+ | LVDS1_D2_P | B29 | LVDS1_D2_P | | | | | | |
| S118 | LVDS1_2- / eDP1_TX2- / DSI1_D2- | LVDS1_D2_N | C28 | LVDS1_D2_N | | | | | | |
| S120 | LVDS1_3+ / eDP1_TX3+ / DSI1_D3+ | LVDS1_D3_P | C29 | LVDS1_D3_P | | | | | | |
| S121 | LVDS1_3- / eDP1_TX3- / DSI1_D3- | LVDS1_D3_N | D28 | LVDS1_D3_N | | | | | | |
| S122 | LCD1_BKLT_PWM | SPDIF_EXT_CLK | AC18 | SPDIF1_EXT_CLK | PWM1_OUT | | GPT1_COMPARE3 | | GPIO5_IO5 | |
| S123 | GPIO13 | GPIO1_IO13 | A6 | GPIO1_IO13 | USB1_OTG_OC | | | | PWM2_OUT | |
| S125 | LVDS0_0+ / eDP0_TX0+ / DSI0_D0+ | LVDS0_D0_P | D29 | LVDS0_D0_P | | | | | | |
| S126 | LVDS0_0- / eDP0_TX0- / DSI0_D0- | LVDS0_D0_N | E28 | LVDS0_D0_N | | | | | | |
| S128 | LVDS0_1+ / eDP0_TX1+ / DSI0_D1+ | LVDS0_D1_P | E29 | LVDS0_D1_P | | | | | | |
| S129 | LVDS0_1- / eDP0_TX1- / DSI0_D1- | LVDS0_D1_N | F28 | LVDS0_D1_N | | | | | | |
| S131 | LVDS0_2+ / eDP0_TX2+ / DSI0_D2+ | LVDS0_D2_P | G29 | LVDS0_D2_P | | | | | | |

*Continued on next page*

Table 14: X1 pin Alternate Functions Primary pins – Secondary pins (Continued)

| MXM3 Pin | SMARC Signal | Soc Signal | Soc Ball Name | ALT0 | ALT1 | ALT2 | ALT3 | ALT4 | ALT5 | ALT6 |
|---|---|---|---|---|---|---|---|---|---|---|
| S132 | LVDS0_2- / eDP0_TX2- / DSI0_D2- | LVDS0_D2_N | H28 | LVDS0_D2_N | | | | | | |
| S134 | LVDS0_CK+ / eDP0_AUX+ / DSI0_CLK+ | LVDS0_CLK_P | F29 | LVDS0_CLK_P | | | | | | |
| S135 | LVDS0_CK- / eDP0_AUX- / DSI0_CLK- | LVDS0_CLK_N | G28 | LVDS0_CLK_N | | | | | | |
| S137 | LVDS0_3+ / eDP0_TX3+ / DSI0_D3+ | LVDS0_D3_P | H29 | LVDS0_D3_P | | | | | | |
| S138 | LVDS0_3- / eDP0_TX3- / DSI0_D3- | LVDS0_D3_N | J28 | LVDS0_D3_N | | | | | | |
| S139 | I2C_LCD_CK | I2C2_SCL | AH6 | I2C2_SCL | ENET_QOS_1588 _EVENT1_IN | USDHC3_CD_B | ECSPI1_MISO | ENET_QOS_1588 _EVENT1_AUX_IN | GPIO5_IO16 | |
| S140 | I2C_LCD_DAT | I2C2_SDA | AE8 | I2C2_SDA | ENET_QOS_1588 _EVENT1_OUT | USDHC3_WP | ECSPI1_SS0 | | GPIO5_IO17 | |
| S141 | LCD0_BKLT_PWM | GPIO1_IO11 | D8 | GPIO1_IO11 | USB2_OTG_ID | PWM2_OUT | | USDHC3_VSELECT | CCM_PMIC_READY | |
| S142 | GPIO12 | GPIO1_IO08 | A8 | GPIO1_IO8 | ENET_QOS_1588 _EVENT0_IN | PWM1_OUT | ISP_PRELIGHT_TRIG_1 | ENET_QOS_1588 _EVENT0_AUX_IN | USDHC2_RESET_B | |
| S145 | WDT_TIME_OUT# | GPIO1_IO02 | B6 | GPIO1_IO2 | WDOG1_WDOG_B | | ISP_FLASH_TRIG_0 | | WDOG1_WDOG_ANY | SJC_DE_B (ALT7) |
| S146 | PCIE_WAKE# | SAI1_RXFS | AJ9 | SAI1_RX_SYNC | SAI5_RX_SYNC | | | ENET1_1588_EVENT0_IN | GPIO4_IO0 | |
| S149 | SLEEP# | NAND_CE0_B | L26 | NAND_CE0_B | QSPI_A_SS0_B | SAI3_TX_DATA0 | ISP_SHUTTER_TRIG_0 | UART3_TX | GPIO3_IO1 | |

# 10 Interface Description

## 10.1 GPIOs

As described in Table 6, the SMARC iMX8M Plus implements 14 dedicated general-purpose input-output (GPIO). Besides these 14 GPIOs, several pins can be used as GPIO if their primary function is not used. For compatibility reasons, it is recommended to use the dedicated GPIOs first.

Table 15: Dedicated GPIOs

| MXM3 Pin | SMARC Signal | Soc Signal | Soc Ball Name | SoC Alternate Function | SoC Function Name |
|---|---|---|---|---|---|
| P108 | GPIO0 / CAM0_PWR# | GPIO_Expander | | ALT0 | GPIO1_IO0 |
| P109 | GPIO1 / CAM1_PWR# | GPIO_Expander | | ALT0 | GPIO1_IO1 |
| P110 | GPIO2 / CAM0_RST# | GPIO_Expander | | ALT0 | GPIO1_IO5 |
| P111 | GPIO3 / CAM1_RST# | GPIO_Expander | | ALT0 | GPIO1_IO6 |
| P112 | GPIO4 / HDA_RST# | SAI1_TXD6 | AC12 | ALT5 | GPIO4_IO18 |
| P113 | GPIO5 / PWM_OUT | GPIO1_IO10 | B7 | ALT0 | GPIO1_IO10 |
| P114 | GPIO6 / TACHIN | SAI3_RXC | AJ18 | ALT5 | GPIO4_IO29 |
| P115 | GPIO7 | GPIO1_IO00 | A7 | ALT0 | GPIO1_IO0 |
| P116 | GPIO8 | GPIO1_IO01 | E8 | ALT0 | GPIO1_IO1 |
| P117 | GPIO9 | GPIO1_IO05 | B4 | ALT0 | GPIO1_IO5 |
| P118 | GPIO10 | GPIO1_IO06 | A3 | ALT0 | GPIO1_IO6 |
| P119 | GPIO11 | GPIO1_IO07 | F6 | ALT0 | GPIO1_IO7 |
| S123 | GPIO13 | GPIO1_IO13 | A6 | ALT0 | GPIO1_IO13 |
| S142 | GPIO12 | GPIO1_IO08 | A8 | ALT0 | GPIO1_IO8 |

## 10.2 USB

As described in Table 6, the SMARC iMX8M Plus implements 5 sets of USB 2.0 signals and two sets of USB 3.2 Super Speed signals. USB OTG and USB Client functionalities are also supported.

Table 16: USB Signal Assignments

| Port | USB 2.0 | USB 3.2 (SS) | OTG / VBUS | Client Capability |
|---|---|---|---|---|
| USB0 | yes | no | yes | yes |
| USB1 | yes | no | no | no |
| USB2 | yes | yes | no | no |
| USB3 | yes | yes | no | no |
| USB4 | yes | no | no | no |
| USB5 | no | no | no | no |

Check the USB Signals section of the Smarc Specification Section 4.7.

## 10.3 Wi-Fi and Bluetooth

The SMARC iMX8M Plus is available with on-module Wi-Fi and Bluetooth interfaces. Optionally, the BTO options (Section 6) includes a version without the Wi-Fi and Bluetooth module. The SMARC module versions make use of the AW-CM276NF Dual-Band Wi-Fi and Bluetooth module from AzureWave.

Features:

- Wi-Fi 802.11a/b/g/n/ac
- Dual-Band 5 GHz and 2.4GHz
- Up to 866.7 Mbps
- 20/40/80 MHz channel bandwidth
- Station/Client Mode, Access Point Mode, Wi-Fi- Direct Mode, and Simultaneous Station and Access point mode
- Bluetooth 5.3 (BR/EDR), BLE
- Murata HSC (MXHP32) connector for the dual external antenna in 2×2 configuration, compatible to IPX/IPEX connector MHF4 series
- Pre-certified for CE (Europe), FCC (United States), IC (Canada), TELEC (Japan), and WPC (India). See https://developer.toradex.com/knowledge-base/wi-fi-accessories-recommended-for-toradex-products.

# 11 Recovery Mode

**Missing Content**
More information about recovery mode will be available on the next release of the datasheet.

# 12 Known Issues

Up-to-date information about all known hardware issues can be found in the errata document, which can be downloaded from our website at https://developer.toradex.com/products/smarc-som-family/modules/smarc-imx8m-plus#tab-erratak nown-issues.

# 13 Technical Specifications

## 13.1 Absolute Maximum Ratings

**Missing Content**
More information about absolute maximum ratings will be available on the next release of the datasheet.

## 13.2 Product Compliance

Up-to-date information about product compliance such as RoHS, CE, UL-94, Conflict Mineral, REACH, etc. can be found on our website at: https://www.toradex.com/support/product-compliance.

## 13.3 Power Consumption

**Missing Content**
More information about power consumption will be available on the next release of the datasheet.

## 13.4 Recommended Operation Conditions

Table 17: Recommended operation conditions

| Symbol | Description | Minimun | Typical | Maximum | Unit |
|---|---|---|---|---|---|
| VCC | Main power supply | 3.0 | 3.3 or 5 | 5.25 | V |
| VCC_BACKUP | RTC power supply | 2.0 | 3.0 | 3.25 | V |

## 13.5 Mechanical Characteristics

The SMARC modules are available in the 82 x 50 mm size, as described in the Section 3. Check the “Module Outline – 82×50mm Module” section of the SMARC specification Section 4.7 on page 13.

### 13.5.1 Sockets for SMARC Modules

The SMARC iMX8M Plus modules uses the MXM3 graphics cards edge connector with 314 pins. Check the “Carrier Connector” section of the SMARC specification Section 4.7 on page 13.

## 13.6 Thermal Specification

**Missing Content**
More information about thermal specification will be available on the next release of the datasheet.

# 14 Device and Documentation Support

## 14.1 Trademarks

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